Universidad de Alcalá
COMISIÓN DE ESTUDIOS OFICIALES DE POSGRADO Y DOCTORADO

ACTA DE EVALUACIÓN DE LA TESIS DOCTORAL

(FOR EVALUATION OF THE ACT DOCTORAL THESIS)

Año académico (*academic year):* 2016/17

DOCTORANDO *(candidate PHD)*: **SANZ ALONSO, INÉS**
D.N.I. / PASAPORTE(*Id.Passport*): ******328W**
PROGRAMA DE DOCTORADO *(Academic Committee of the Programme)*: **D332 DOCTORADO EN ELECTRÓNICA:SISTEMAS ELECTRÓNICOS AVANZADOS.SISTEMAS INTELIGEN**
DEPARTAMENTO DE *(Department)*: **ELECTRÓNICA**
TITULACIÓN DE DOCTOR EN *(Phd title)*: **DOCTOR/A POR LA UNIVERSIDAD DE ALCALÁ**

En el día de hoy 16/06/17, reunido el tribunal de evaluación, constituido por los miembros que suscriben el presente Acta, el aspirante defendió su Tesis Doctoral **con Mención Internacional** (*In today assessment met the court, consisting of the members who signed this Act, the candidate defended his doctoral thesis with mention as International Doctorate),* elaborada bajo la dirección de (*prepared under the direction of*) EMILIO JOSÉ BUENO PEÑA // FRANCISCO JAVIER RODRÍGUEZ SÁNCHEZ.

Sobre el siguiente tema *(Title of the doctoral thesis)*: *COMPARATIVE ANALYSIS OF MULTILEVEL CONVERTERS FOR MEDIUM-VOLTAGE APPLICATIONS*

Finalizada la defensa y discusión de la tesis, el tribunal acordó otorgar la CALIFICACIÓN GLOBAL[2] de (**no apto, aprobado, notable** y **sobresaliente)** *(After the defense and defense of the thesis, the court agreed to grant the GLOBAL RATING (fail, pass, good and excellent)*: SOBRESALIENTE

Alcalá de Henares, a ...16.... de ....junio.....de 2017

Fdo. *(Signed)*: JOSÉ IGNACIO LEÓN GALVÁN Fdo. *(Signed)*: FRANCISCO HUERTA SÁNCHEZ Fdo. *(Signed)*: FRANCISCO DANIEL FREIJEDO FERNÁNDEZ

FIRMA DEL ALUMNO (candidate's signature),

Fdo. *(Signed)*: .....INÉS SANZ ALONSO

Con fecha 29 de junio de 2017 la Comisión Delegada de la Comisión de Estudios Oficiales de Posgrado, a la vista de los votos emitidos de manera anónima por el tribunal que ha juzgado la tesis, resuelve:

☐ Conceder la Mención de "Cum Laude"
☒ No conceder la Mención de "Cum Laude"

La Secretaria de la Comisión Delegada

[2] La calificación podrá ser "**no apto**" "**aprobado**" "**notable**" y "**sobresaliente**". El tribunal podrá otorgar la mención de "cum laude" si la calificación global es de sobresaliente y se emite en tal sentido el voto secreto positivo por unanimidad. (*The grade may be "**fail**" "**pass**" "**good**" or "**excellent**". The panel may confer the distinction of "cum laude" if the overall grade is "Excellent" and has been awarded unanimously as such after secret voting.).*

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En aplicación del art. 14.7 del RD. 99/2011 y el art. 14 del Reglamento de Elaboración, Autorización y Defensa de la Tesis Doctoral, la Comisión Delegada de la Comisión de Estudios Oficiales de Posgrado y Doctorado, en sesión pública de fecha 29 de junio, procedió al escrutinio de los votos emitidos por los miembros del tribunal de la tesis defendida por *SANZ ALONSO, INÉS*, el día 16 de junio de 2017, titulada *COMPARATIVE ANALYSIS OF MULTILEVEL CONVERTERS FOR MEDIUM-VOLTAGE APPLICATIONS*, para determinar si a la misma se le concede la mención "cum laude", arrojando como resultado, 3 votos en contra.

Por lo tanto, la Comisión de Estudios Oficiales de Posgrado **resuelve no otorgar la Mención de "cum laude"** a dicha Tesis.

Alcalá de Henares, 11 de julio de 2017
EL PRESIDENTE DE LA COMISIÓN DE ESTUDIOS
OFICIALES DE POSGRADO Y DOCTORADO

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DILIGENCIA DE DEPÓSITO DE TESIS.

Comprobado que el expediente académico de D./Dª INÉS SANZ ALONSO reúne los requisitos exigidos para la presentación de la Tesis, de acuerdo a la normativa vigente, y habiendo presentado la misma en formato: ☒ soporte electrónico ☐ impreso en papel, para el depósito de la misma, en el Servicio de Estudios Oficiales de Posgrado, con el nº de páginas: 234 se procede, con fecha de hoy a registrar el depósito de la tesis.

Alcalá de Henares a 20 de abril de 2017

Rosa Carrillo Salas

Fdo. El Funcionario

Universidad de Alcalá

Departamento de Electrónica

Doctorado en Electrónica: Sistemas Electrónicos Avanzados. Sistemas Inteligentes.

PhD Thesis

COMPARATIVE ANALYSIS OF MULTILEVEL CONVERTERS FOR MEDIUM-VOLTAGE APPLICATIONS

Inés Sanz Alonso

Supervisors: Dr. Emilio José Bueno Peña

Dr. Francisco Javier Rodríguez Sánchez

2017

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Dr. Francisco Javier Rodríguez Sánchez, Profesor Catedrático de la Universidad Alcalá,

INFORMAN: Que la Tesis Doctoral titulada "**Comparative Analysis of Multilevel Converters for Medium Voltage Applications**" presentada por Dª. Inés Sanz Alonso, y realizada bajo la dirección de los doctores D. Emilio José Bueno Peña y D. Francisco Javier Rodríguez Sánchez, dentro del campo de la aplicación de los convertidores multinivel para aplicaciones de media tensión, reúne los méritos de calidad y originalidad para optar al Grado de Doctor.

Alcalá de Henares, 30 de Marzo de 2017

UNIVERSIDAD DE ALCALÁ DEPARTAMENTO DE ELECTRÓNICA EDIFICIO POLITÉCNICO

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INFORMA: Que la Tesis Doctoral titulada "**Comparative Analysis of Multilevel Converters for Medium Voltage Applications**" presentada por Dª. Inés Sanz Alonso, y dirigida por los doctores D. Emilio José Bueno Peña y D. Francisco Javier Rodríguez Sánchez, cumple con todos los requisitos científicos y metodológicos, para ser defendida ante un Tribunal, según lo indicado por la Comisión Académica del Programa de Doctorado.

Alcalá de Henares, 30 de Marzo de 2017

Fdo. Sira Elena Palazuelos Cagigas

ABSTRACT

The electric energy demand has been steadily growing during the last century, and all forecasts indicate that it will keep growing in the following years. Within this frame, and due to all the problems that this demand increase generate in the environment, it is necessary improving the current techniques of electric energy conversion and transmission in order to increase the whole system efficiency. On the other hand, it is also necessary increasing the renewable energy resources exploitation through more efficient generation systems.

According to these lines, the power electronics systems that have been installed in the last decades allowed to obtain better efficiency from the renewable natural resources like the wind or the solar power. These systems have also notably improved the quality of the power supplied, reducing the losses through what are known as power quality applications.

Power converters are currently essential in any power electronics system. Within them, the multilevel converters specially suppose a breakthrough compared with the classical two-level converters, as they allow obtaining voltage and current signals with lower harmonic content, what means fewer losses in high-power medium-voltage applications.

In this Thesis a comparative study of some multilevel converter topologies normally used in high-power medium-voltage applications is done. The objective is analyzing in detail each topology and comparing it with the rest following different criteria, with the aim to know the advantages and drawbacks of each one and to realize which one is more suitable for each application.

RESUMEN

El consumo de energía eléctrica no ha parado de crecer en el último siglo, y todas las previsiones apuntan a que lo va a seguir haciendo en los próximos años. Dentro de este marco, y debido a los problemas que este incremento en el consumo genera en el medio ambiente, se hace necesario mejorar las técnicas actuales de conversión y transmisión de energía eléctrica para incrementar la eficiencia del sistema completo. Por otro lado, se hace necesario incrementar el aprovechamiento de los recursos energéticos renovables mediante sistemas de generación más eficientes.

Siguiendo esas líneas, los sistemas de electrónica de potencia que se han ido instalando en las últimas décadas han permitido obtener un mejor aprovechamiento de los recursos naturales como el viento o la luz solar, y además han mejorado notablemente la calidad de la energía suministrada, reduciendo las pérdidas a través de lo que se conoce como aplicaciones de "*power quality*".

Los convertidores de potencia son actualmente indispensables en cualquier sistema de electrónica de potencia. Dentro de ellos, especialmente los convertidores multinivel suponen un gran avance respecto a los convertidores clásicos de dos niveles, ya que permiten obtener señales con menos contenido armónico, lo que se traduce en menos pérdidas en los sistemas de media tensión y alta potencia.

En esta Tesis se hace un estudio comparativo de varias topologías de convertidores multinivel que suelen utilizarse en aplicaciones de media tensión y alta potencia. El objetivo es analizar pormenorizadamente cada topología y compararla con las demás en base a diferentes criterios, con el propósito de conocer los puntos fuertes y débiles de cada una y discernir cuál es más adecuada para cada aplicación.

AGRADECIMIENTOS

Esta Tesis es fruto de los trabajos realizados por su autora dentro del grupo de investigación GEISER durante los últimos cuatro años y medio. Durante este periodo han sido muchas personas las que han influido en la consecución de dicho trabajo. Sirvan estas palabras como reconocimiento para todas ellas aunque no sean mencionadas expresamente.

En primer lugar me gustaría dar las gracias a los supervisores de mi trabajo, los doctores Emilio Bueno y Fco. Javier Sánchez, por tomarse la molestia de revisar todo este trabajo, y poner a mi disposición los recursos del grupo de investigación. Agradezco especialmente tu labor, Emilio, por todo lo que me has enseñado, la paciencia que has tenido conmigo, y la confianza que depositaste en mí el día que me fichaste (de verdad, doy gracias por haberme encontrado de casualidad aquel día contigo).

También quiero agradecer a todos los compañeros con los que he coincidido en el grupo de investigación, por los conocimientos compartidos, o simplemente por los buenos ratos que hemos pasado trabajando (a la mente me llegan recuerdos de charlas con los doctores Mario Rizo o Rafa Peña…). Me gustaría agradecer especialmente a Miguel Moranchel todo lo que me ha enseñado, el haber tenido una actitud tan positiva en el trabajo, y el haberme prestado su ayuda en innumerables ocasiones; sin duda, ha sido un placer tenerte como compañero durante estos años.

Agradezco también la compañía y los buenos ratos pasados con el resto de compañeros de otros grupos de investigación, especialmente con Laura, Susel, y Marco, y con los compis de café: Luis, Diego, Germán y CJ.

Por otro lado quiero agradecer el apoyo que me ha brindado mi familia: agradezco a mi padre que luchara por vivir y poder estar hoy a mi lado, y que me animara en todo momento a avanzar más y más; doy gracias a mi madre por haber sido mi mayor fan y haberme hecho

creer en mí misma, aunque perdiera la batalla su recuerdo y sus enseñanzas seguirán vivas para siempre; doy gracias a mis hermanos por ser como son, por estar a mi lado, por traer a mi vida a mis sobrinas que han supuesto una alegría tan grande… Aunque todavía sean pequeñas, espero que algún día entiendan lo que significan para mí y lo que han ayudado en este trabajo. Haré mención especial a mi hermana Bea, la primera doctora Sanz de nuestra familia, por todo su apoyo y por haberme puesto el listón tan alto y animarme siempre a superarlo. También quiero agradecer a Javi el haber estado a mi lado desde hace tanto, y su disposición a ayudarme en cualquier situación. También agradezco al resto de mi familia, a mis tíos y primos, todo su cariño y apoyo.

Por último quiero dedicar unas palabras de agradecimiento a todos los amigos que han estado pendientes de la evolución de este trabajo, animándome en los malos ratos, y procurándome un poco de necesaria distracción de cuando en cuando. A todos vosotros, gracias.

GLOSSARY

AC	Alternating current
ANPC	Active neutral point-clamped
APOD	Alternative phase opposite disposition
CHB	Cascaded H-bridge
DC	Direct Current
DNPC	Diode neutral point-clamped
DPF	Displacement power factor
DSP	Digital signals processor
EMF	Electromotive force
FACTS	Flexible AC transmission system
FOC	Field oriented control
FPGA	Field programmable gate array
GTO	Gate turn-off (thyristor)
HV	High voltage
HVDC	High voltage direct current
IGBT	Insulated gate bipolar transistor
IGCT	Integrated gate-commutated thyristor
IM	Induction machine / induction motor
IPD	In phase disposition

LV	Low voltage
MMC	Modular multilevel converter
MOSFET	Metal-oxide-semiconductor field-effect transistor
MV	Medium voltage
NLM	Nearest-level modulation
NPC	Neutral point-clamped
PCC	Point of common coupling
PF	Power factor
PI	Proportional-integral
PLL	Phase locked loop
POD	Phase opposite disposition
PWM	Pulse-width modulation
SCR	Silicon controlled rectifier
SHE	Selective harmonic elimination
SISO	Single input, single output
SM	Submodule
SPWM	Sinusoidal pulse-width modulation
STATCOM	STATtic COMpensator
SVM	Space vector modulation
THD	Total harmonic distortion
VSC	Voltage source converter
WTHD	Weighted total harmonic distortion
ZOH	Zero order hold

SUMMARY OF FIGURES AND TABLES

Summary of figures

Summary of tables

A Sofía y Marisa, por llegar a mí para ser mis salvadoras, mi razón de vivir, mi alegría.

A Ti, que ya no puedes leer estas líneas. No te fuiste del todo, sigues en mí.

CONTENTS

Chapter 1: INTRODUCTION

1.1. Introduction

According to some organizations like the World Energy Council (WEC) or the U.S. Energy Information Administration (EIA), the World electric energy demand will continue growing in the next years [1], [2]. Of course, this growth in the demand must be corresponded with an increase in the energy generation. As an example, the forecast for world electricity generation growth for the year 2040 is 69 %: from 21.6 trillion (US trillion = 10^{12}) kilowatt-hours in 2012 to 25.8 trillion kWh in 2020 and 36.5 trillion kWh in 2040 [3]. This growth will be more evident in non-OECD countries (Figure 1.1), as in OECD countries energy markets are well established and electricity consumption patterns are mature.

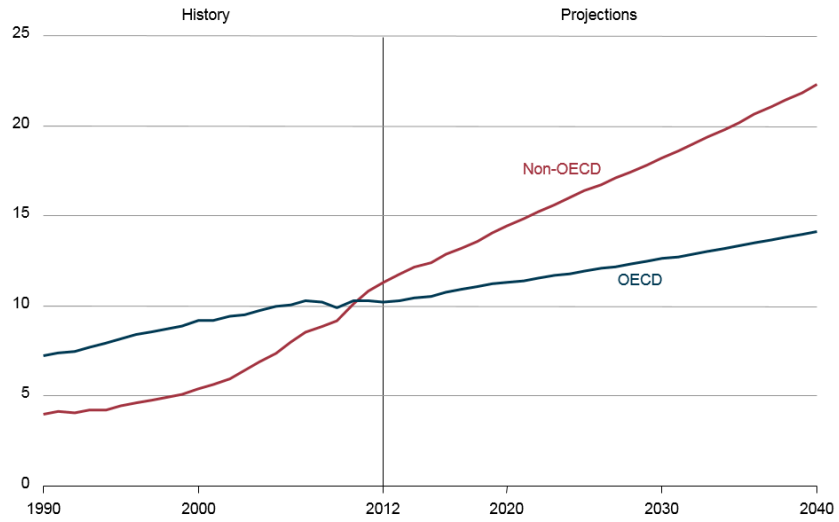


Figure 1.1. OECD and non-OECD countries electricity generation from 1990 to 2040 in trillion of kWh (US trillion = 10^{12}) [3].

With this scenario and having in mind the concerns related to the environment care, the electricity generation systems should tend to use renewable primary energies as far as possible, be CO_2 generation free, be safe for the environment and produce few or no residues, and be independent of political or economic conflicts. At the same time, power management systems should avoid losses improving the efficiency.

Far to reduce the generation with fossil fuels, the expectation of power generation for the next years is to maintain the use of these primary energies and gently increasing the production with renewable energies. The representation of the electricity generation forecast for the next years can be seen in Figure 1.2.

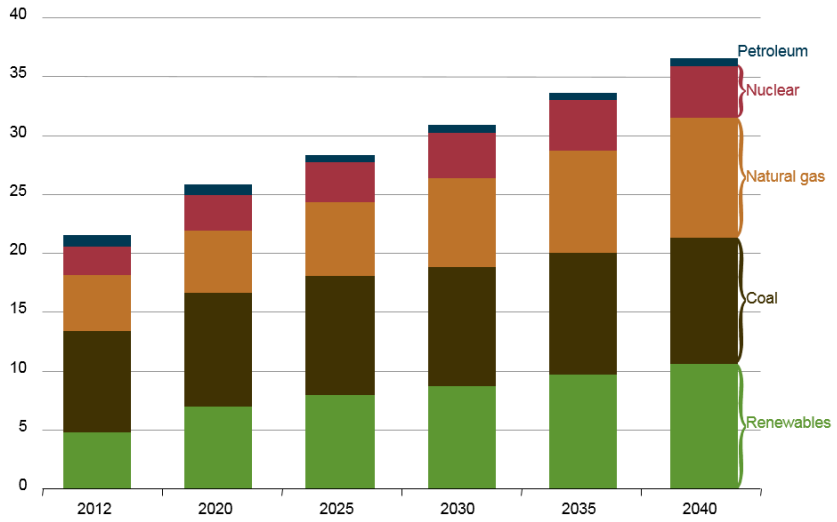


Figure 1.2. World electricity generation forecast by fuel in trillion kWh (US trillion = 10^{12}) [3].

As the power demand will keep growing and that not all the generation sources are clean or renewable, there is necessity to control correctly the electric systems in order to integrate the renewable resources, minimize the power losses, and improve the energy quality. The tendency is to do these tasks through high-power medium-voltage systems.

Following this premise, nobody can imagine smart medium-voltage applications without power converters, both terms go hand in hand. So, the use of power converters is a requirement in medium-voltage (MV) power applications such as motor drives, flexible AC transmission systems (FACTS), renewable energy resources integration, high voltage DC (HVDC) transmissions, etc. Since power converters are essential for those applications, it is necessary to choose the more suitable alternative for each case.

On the other hand, there is an essential component in the power converters, without which they could not have been conceived: the power switching device. Nowadays all the switching devices used are semiconductor-based. So much so, that semiconductor devices can be considered as the back-bone of power converters and the development of the last ones has been linked to that of the first ones.

The evolution of switching devices from their origins to the actual devices has been awesome. This evolution has always been aimed to resemble an ideal switch, so historically new devices improved the characteristics of previous ones. Figure 1.3 shows the development of power switching devices toward the concept of ideal switch.

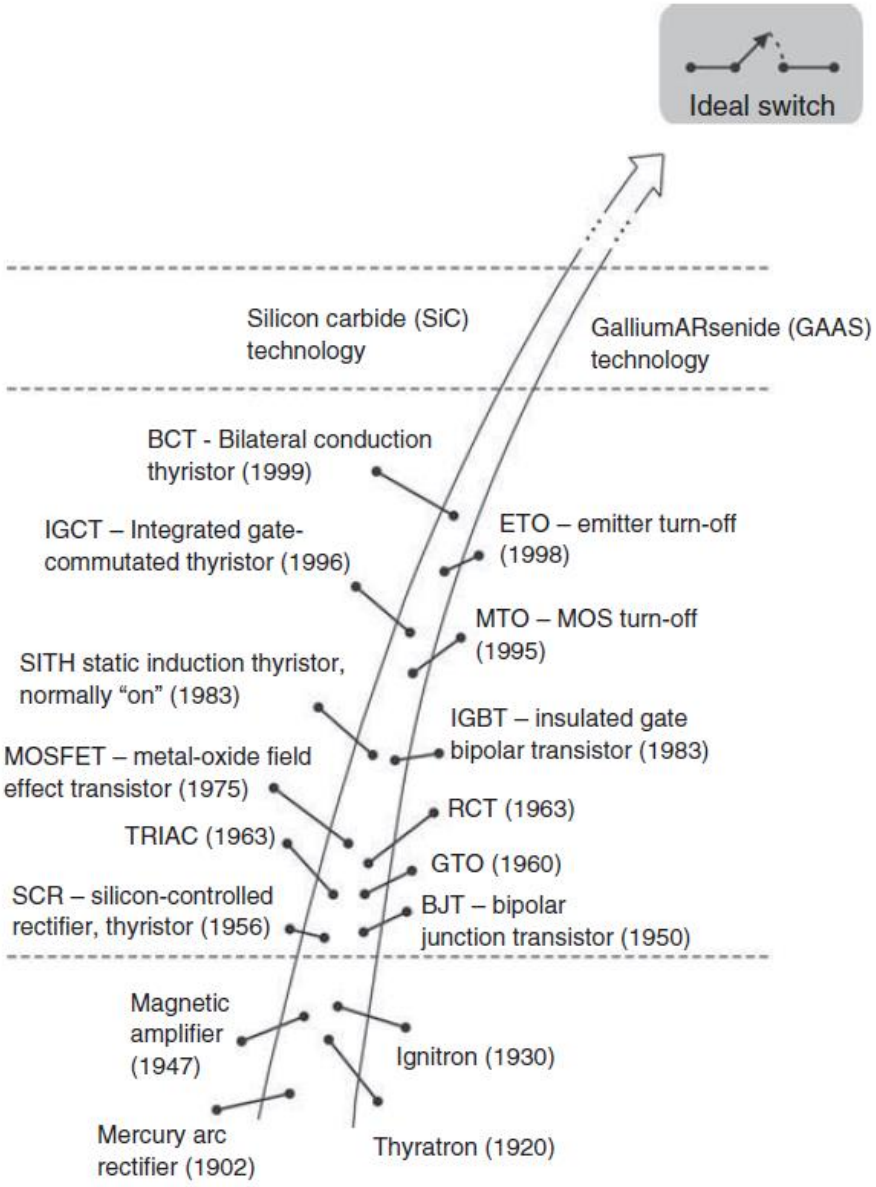


Figure 1.3. Evolution of power switching devices toward the concept of ideal switch [4].

The characteristics to be evaluated in a switching device are the operating frequency, the blocking voltage, and the drive current. In this way, an ideal switch would have infinite operating frequency, infinite blocking voltage, drop voltage equal to zero (when On), and drive current equal to zero when Off and infinite when On. In such conditions there would not be any conduction or switching losses in the switch.

As the commercial devices are not ideal yet, and probably they never will be, for each application the correct one should be chosen according with each system requirements. Figure 1.4 shows a comparison between different kinds of devices depending on their frequency and

power ranges, and the maximum current and voltage they can manage. As it was said, each kind of semiconductor device is better for a specific application, Figure 1.5 summarizes the most used types of devices for the main current applications.

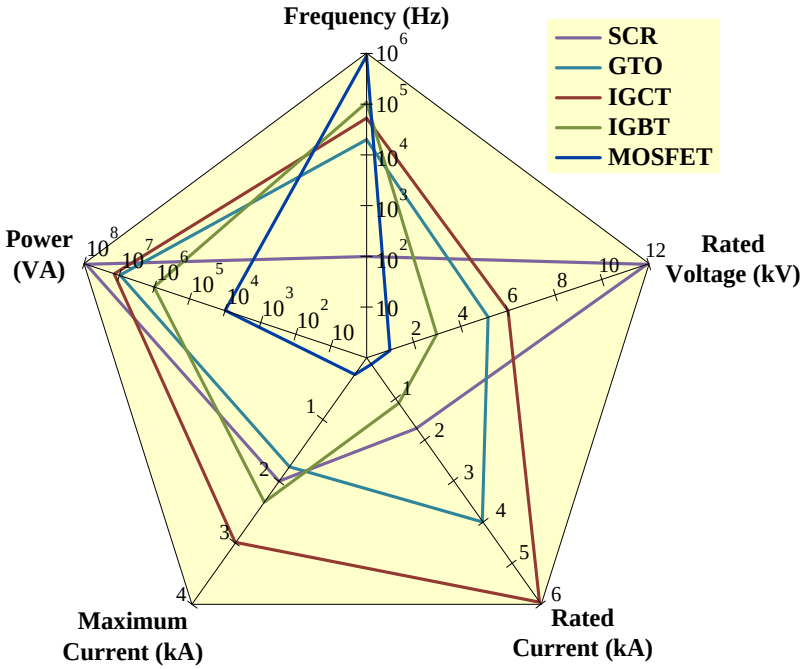


Figure 1.4. Power devices comparison depending on their main parameters [5],[6].

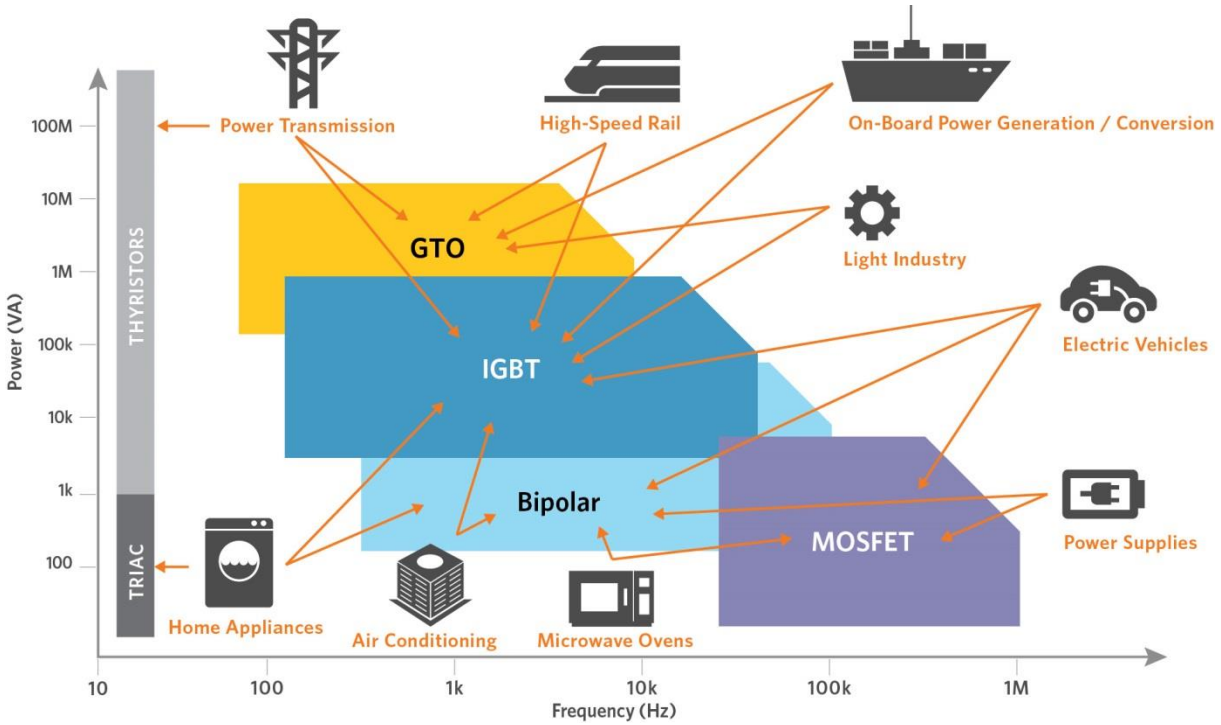


Figure 1.5. Classification of power devices attending to their power and frequency ranges, and main application where they are used [7].

But, although the best device is chosen, the trend is to use associated devices in order to allow the management of more voltage, more current, and to get higher equivalent switching frequency from the point of view of the grid side, maintaining the individual switching frequency for the devices. This fact gives rise to another type of converters that are known as multilevel power converters.

Multilevel converters suppose another kind of topologies that generates cleaner voltage and current waveforms, reducing the harmonic content. They allow some high-power applications that are not achievable for the conventional two-level converter. The term 'multilevel' defines topologies with more than one power source [8], and hence with the capability of have more than two voltage levels at the output (see Figure 1.6)

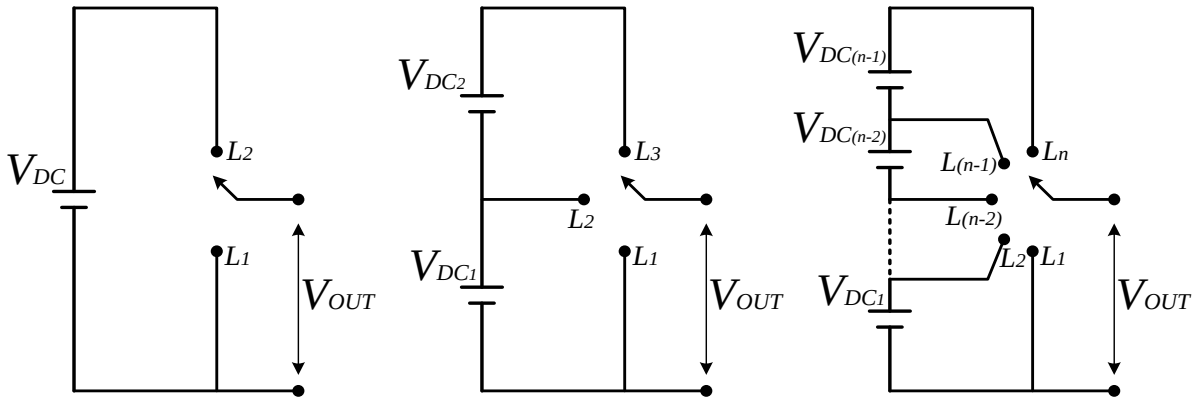


Figure 1.6. Illustration of generic two-level converter a), three-level converter b), and n-level converter c).

Moreover, with multilevel converters more accurate voltage signals can be achieved, and with less harmonic content as can be seen in Figure 1.7. This figure shows how the voltage waveform (in blue) is slowly going near to the sinusoidal waveform (in red) as the number of levels increases. This fact makes the harmonic content decrease following the same tendency.

So, those are the main reasons why the power multilevel converters have been increasingly used in high-power medium-voltage applications: they can produce cleaner voltage signals reducing the harmonic content; and the managed voltage is shared among a higher number of devices, and hence the election of devices is not so critical for the same voltage level.

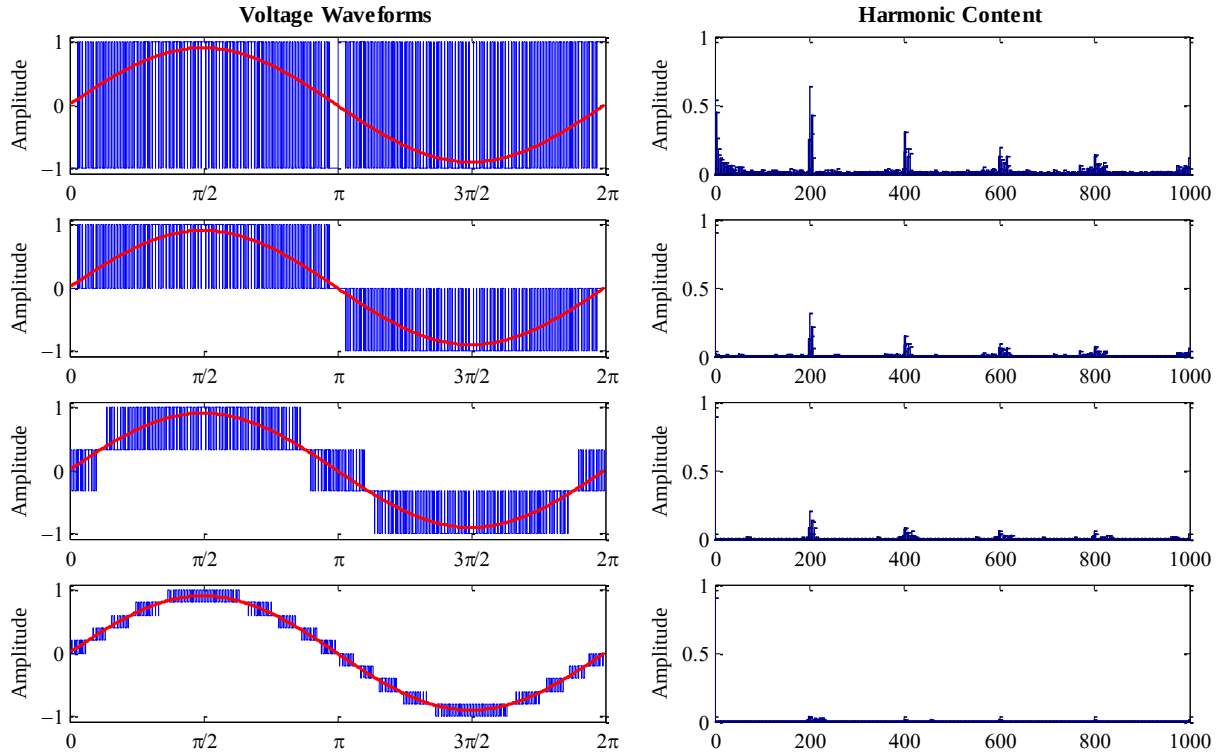


Figure 1.7. Example of multilevel signals (left) and their corresponding harmonic content (right). From top to bottom: 2-levels waveform, 3-levels,4-levels, and 11-levels.

1.2. Objectives of this thesis

Although there are some works that study the multilevel topologies, there are still many analyses that can be done, especially in relation to their use in medium voltage applications. In this line, in this thesis four multilevel topologies are studied: Diode Neutral Point-Clamped (DNPC), Active Neutral Point-Clamped (ANPC), Cascaded H-Bridge (CHB), and Modular Multilevel Converter (MMC). The general aim of this Thesis is comparing these four topologies and their behaviors when they are integrated in different medium voltage applications, in order to identify the advantages and disadvantages of each one of them.

To achieve the general aim, the following objectives will be met:

- Exhaustive analysis of each one of the mentioned topologies and their operation.
- Detailed analysis of the pulse-width modulation techniques typically employed in medium voltage applications, paying special attention to the modulation based on selective harmonic elimination for each one of the four topologies.
- Alternative proposal to choose the zero states in ANPC topology when the SHE modulation is used.
- Comparative analysis of each topology operation under conditions of fault in the devices assuring the minimum distortion as possible. In this line, it is done a

proposal of neutral-shift fault-tolerant method that balances the phase-to-phase voltages when there is a fault in a modular converter like CHB. This point supposes one of the main contributions of this Thesis.

- Detailed analysis of the medium voltage applications in which each one of the explained topologies is more commonly used. Also it will be analyzed which topology is more suitable for each application.

- Testing process of the modulation and control methods over prototypes of the different topologies analyzed in this Thesis. One of the prototypes (the CHB) has been development completely during this Thesis and the others were development previously in the research group.

1.3. Structure of this Thesis

The organization of this Thesis has been done as follows:

- The second chapter makes a background about multilevel topologies, modulation techniques and fault tolerant methods.

- Chapter three describes the diode neutral point-clamped converter and the active neutral point-clamped converter as well as the most used modulation methods applied to these topologies.

- The forth chapter is about the cascade H-bridge converter, and in this chapter in addition to its typical modulation methods, the possibilities to fault-tolerant operation are explained.

- In chapter five it is made a description of the modular multilevel converter and its modulation techniques and fault-tolerant options.

- Chapter six describes the laboratory prototypes used to test the algorithms and modulation methods explained in this work.

- The seventh chapter contains a complete comparison of the four studied topologies that include theoretical data, simulation results, and experimental results of the tests carrying out during this work.

- The conclusions and future works are summarized in chapter eight.

In addition to these eight chapters, there are three appendixes that explain the basis of multi-pulse transformers (Appendix A), STATCOM systems (Appendix B), and induction motors and their control techniques (Appendix C).

1.4. Projects related with this Thesis

The work developed for this Thesis is related to some projects that have had public and private funding. Those projects are the following:

- ENE2011-28527-C04-02, "*Applications of HVDC-VSC to electric power systems with special attention to multi-terminal operation*", funded by the Spanish Ministry of Economy and Competitiveness.
  Some of the studies about the modular multilevel converter that are related with the work of this Thesis are also included in this project.

- PRICAM project (S2013-ICE-2933), "*Programa redes eléctricas inteligentes de la comunidad de Madrid*", funded by the Regional Government of Madrid (Spain).
  In this project they are included some of the conclusions contained in this Thesis about the medium voltage operation of multilevel converters used in applications like FACTs. Specifically, those conclusions are part of the first objective of the project: "Integración de dispositivos electrónicos de potencia, como FACTs, SSTs y conexiones HVDC en las redes eléctricas inteligentes".

- CONPOSITE project (ENE2014-57760-C2-2-R), "*Convertidores de potencia para optimizar la operacion de sistemas hibridos HVDC-VSC multiterminal/HVAC*", funded by the Spanish Ministry of Economy and Competitiveness.
  Some of the studies about the modular multilevel converter that are in this Thesis, are also included in this project.

- "*Desarrollo de un variador de velocidad para motores eléctricos de media tensión*", funded by the company *Sedecal Control*, from 2012 to 2016.
  This author has taken part on this Project with the studies related to the fault-tolerant operation of cascaded H-bridge converters.

1.5. Related Papers

In this section the journal and conference publications related with this thesis that have been written by this author are listed.

Journal publications:

1- Moranchel, M., Huerta, F., Sanz, I., Bueno, E., & Rodríguez, F. J. (2016). A Comparison of Modulation Techniques for Modular Multilevel Converters. Energies, 9(12), 1091.

This work presents a comparison of three different modulation techniques applied to modular multilevel converters: SPWM, SVM, and NLM, analyzing the particularities and implementation of each one of them. In addition, the paper presents and compares the digital implementation of the three modulation methods in a FPGA. The proposed

approaches are validated using a real processing platform and experimentally evaluated in a real high-power six-level MMC.

2- Moranchel, M., Bueno, E., Sanz, I., & Rodríguez, F. J. (2017). New Approaches to Circulating Current Controllers for Modular Multilevel Converters. Energies, 10(1), 86.

This paper focuses on the analysis and suppression of circulating currents in a MMC using two algorithms for tracking of harmonics, though the use of resonant controllers and repetitive controllers. Both controllers are analyzed and simulations results are presented. Moreover, the controllers have been tested and validated for a three phase MMC operating as an inverter, using a real MMC prototype that is controlled with a processing platform based on Zynq by Xilinx, and designed to control large multilevel converters. These results prove the feasibility of the proposed method.

Pending publications:

1- Sanz, I., Moranchel, M., Bueno, E., & Rodríguez, F. J., Comparison of medium voltage modular multilevel topologies working in power quality applications.

In this publication the intention is to analyze in detail the behavior of cascaded H-bridge converters and modular multilevel converters working in power quality applications, with the aim to check if these topologies, which were initially designed for other purposes, are suitable for other applications. The considerations that should be taken into account are also studied.

2- Sanz, I., Bueno, E., Moranchel, M., & Rodríguez, F. J., Analysis of multilevel converters operation using selective harmonic elimination.

The aim of this publication is determining the peculiarities that should be met when selective harmonic elimination is implemented in multilevel topologies such as modular multilevel converters, or cascaded H-bridge converters.

3- Sanz, I., Bueno, E., Moranchel, M., & Rodríguez, F. J., Comparison of multilevel topologies used in MV applications.

In this paper it is contained a summary of all contributions presented in this Thesis about the different modulation methods used for the studied topologies. Also it is included a comparative analysis of these converters operation working with SHE in open loop, and the considerations that should be taken into account for the controllers tuning when this modulation method is employed.

Conference publications:

1- Sanz, I., Moranchel, M., Bueno, E. J., & Rodriguez, F. J. (2016, October). Analysis of medium voltage modular multilevel converters for FACTS applications. In Industrial Electronics Society, IECON 2016-42nd Annual Conference of the IEEE (pp. 6459-6464). IEEE.

2- Sanz, I., Bueno, E. J., Moranchel, M., & Rodríguez, F. J. (2016, June). Stair-case selective harmonic elimination for a nine-levels cascaded H-bridge converter. In Power Electronics for Distributed Generation Systems (PEDG), 2016 IEEE 7th International Symposium on (pp. 1-4). IEEE.

3- Sanz, I., Moranchel, M., Bueno, E. J., & Rodríguez, F. J. (2016, June). Nine-levels cascaded H-bridge converter prototype for FACTS applications. In Power Electronics for Distributed Generation Systems (PEDG), 2016 IEEE 7th International Symposium on (pp. 1-4). IEEE.

4- Sanz, I., Bueno, E. J., Moranchel, M., & Rodríguez, F. J. (2015, November). Fault-tolerant cascaded H-bridge converter for an induction motor drive. In Industrial Electronics Society, IECON 2015-41st Annual Conference of the IEEE (pp. 003980-003985). IEEE.

5- Sanz, I., Bueno, E. J., Moranchel, M., & Rodríguez, F. J. (2015, June). Analytical fault-tolerant method for cascaded H-bridge converters. In Power Electronics for Distributed Generation Systems (PEDG), 2015 IEEE 6th International Symposium on (pp. 1-5). IEEE.

6- Sanz, I., Bueno, E. J., Rodríguez, F. J., Moranchel, M., & Mingo, J. (2014, October). Selective harmonic elimination for a NPC converter using modified carrier signals. In Industrial Electronics Society, IECON 2014-40th Annual Conference of the IEEE (pp. 1766-1771). IEEE.

7- Sanz, I., Bueno, E.J., Rodríguez, F.J., & Moranchel, M. (2014, May). New Proposal of Switching Strategies for Loss Balancing in ANPC Converters. In Modeling and Simulation of Electric Machines, Converters and Systems, 2014. ELECTRIMACS 2014. 11th International Conference (p. 481 486). IMACS.

8- Sanz, I., Bueno, E. J., Rodriguez, F. J., Moranchel, M., & Mayor, A. (2013, November). Modulation and balancing methods for a NPC converter connected to the grid in a medium voltage application: a STATCOM system. In Industrial Electronics Society, IECON 2013-39th Annual Conference of the IEEE (pp. 1043-1048). IEEE.

9- Moranchel, M., Sanz, I., Bueno, E. J., Huerta, F., & Rodriguez, F. J. (2016, October). Circulating current elimination in Modular Multilevel Converter with repetitive controllers. In Industrial Electronics Society, IECON 2016-42nd Annual Conference of the IEEE (pp. 6476-6481). IEEE.

10- Moranchel, M., Bueno, E. J., Rodriguez, F. J., & Sanz, I. (2016, June). Selective Harmonic Elimination modulation for Medium Voltage Modular Multilevel Converter. In Power Electronics for Distributed Generation Systems (PEDG), 2016 IEEE 7th International Symposium on (pp. 1-6). IEEE.

11- Moranchel, M., Bueno, E. J., Rodriguez, F. J., & Sanz, I. (2016, June). Circulating current elimination in Modular Multilevel Converter with resonant controllers. In Power Electronics for Distributed Generation Systems (PEDG), 2016 IEEE 7th International Symposium on (pp. 1-6). IEEE.

12- Moranchel, M., Sanchez, F. M., Bueno, E. J., Rodriguez, F. J., & Sanz, I. (2015, November). Six-level modular multilevel converter prototype with centralized hardware platform controller. In Industrial Electronics Society, IECON 2015-41st Annual Conference of the IEEE (pp. 003863-003868). IEEE.

13- Moranchel, M., Sanz, I., Bueno, E. J., & Rodriguez, F. J. (2015, November). Comparative of modulation techniques for modular multilevel converter. In Industrial Electronics Society, IECON 2015-41st Annual Conference of the IEEE (pp. 003875-003880). IEEE.

14- Moranchel, M., Bueno, E. J., Rodriguez, F. J., & Sanz, I. (2015, June). Implementation of nearest level modulation for modular multilevel converter. In Power Electronics for Distributed Generation Systems (PEDG), 2015 IEEE 6th International Symposium on (pp. 1-5). IEEE.

15- Moranchel, M., Bueno, E. J., Rodriguez, F. J., & Sanz, I. (2014, October). Novel capacitor voltage balancing algorithm for modular multilevel converter. In Industrial Electronics Society, IECON 2014-40th Annual Conference of the IEEE (pp. 4697-4701). IEEE.

Chapter 2: BACKGROUND

As it was mentioned in the first chapter, the work of this Thesis is focused on doing a comparative study of some multilevel converter topologies, with the aim to identify the benefits and drawbacks of each one.

In the present chapter a review of the most important previous works about multilevel converter topologies, the principal modulation methods, and the fault-tolerant possibilities is done. And after that, the main contributions of this Thesis in those areas are detailed.

2.1. Overview

2.1.1. Multilevel topologies overview

Multilevel converters were proposed as a solution for high-voltage, high-power applications such as FACTS, electric vehicles, renewable resources, or induction motor drives, due to they can reach high voltage and reduce the harmonic content in their output signals.

As the term ‘multilevel’ includes all the topologies that can supply an output voltage signal with more than two voltage levels, it is necessary to do a tighter classification of the different topologies.

Figure 2.1 shows a classification of the multilevel topologies attending to the type of DC supply. On one hand there are converters that work with a single DC source, and on the other it is the cascaded H-bridge converter that works with multiple isolated DC sources, which can be equal or unequal generating in this way a sub-classification. Different options can be found within the converters that work with a single DC source, as the modular multilevel converter topology that is the most recent and promising topology, the flying

capacitors converter, and the clamped topologies, which are sub-classified depending on the number of levels (the most used are the three-level that are known as neutral point clamped converters), and also depending on the type of clamped device used: if it is a diode the topology is known as Diode Neutral Point Clamped, and if it is an active device it would lead to an Active Neutral Point Clamped.

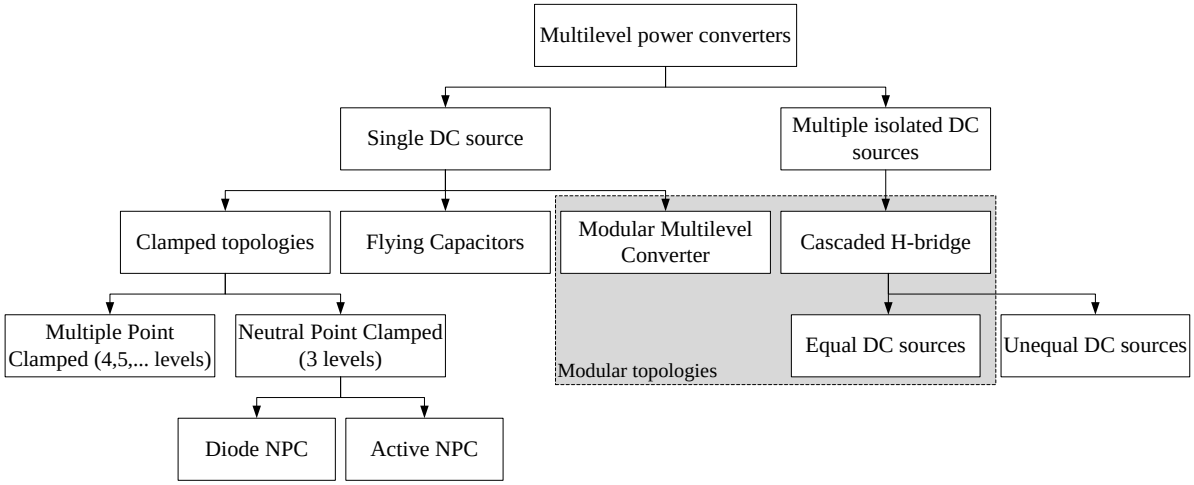


Figure 2.1. Classification of multilevel power converters.

According to that, in this Thesis a comparative study about some of these topologies is done, as it was observed that there is a lot of documentation of each topology analyzed separately, but there is a lack of studies that compare them. The chosen topologies are the three-level neutral point clamped topologies (NPC) in its two variants: the diode neutral point clamped (DNPC) converter, and the active neutral point clamped (ANPC) converter; also two modular topologies will be studied: the cascaded H-bridge (CHB) converter; and the modular multilevel converter (MMC).

Neutral Point-Clamped topologies: DNPC and ANPC

The 3-level Diode Neutral Point-Clamped (DNPC) converter, which was firstly described in [9], and it and its evolution (the Active NPC) have been widely used in many medium voltage applications [10], [11].

Both topologies are three-level, what means that each of their phases can generate three voltage levels: V_d /2, 0, and $-V_d$ /2, usually represented by the switching states named P, 0, and N.

Figure 2.2 shows one phase of these two topologies, and in that figure it can be seen that both topologies are very similar: they have four active devices (S_1, S_2, S_3, and S_4) in series connected between the terminals of the DC supply (V_d), and two devices clamped to the mid-point of the DC source or also known as neutral point. The difference between these two topologies lies in the type of device that is clamped to the neutral point: diodes on the first case (D_{01}, D_{02}), and active devices on the second case (S_5, S_6).

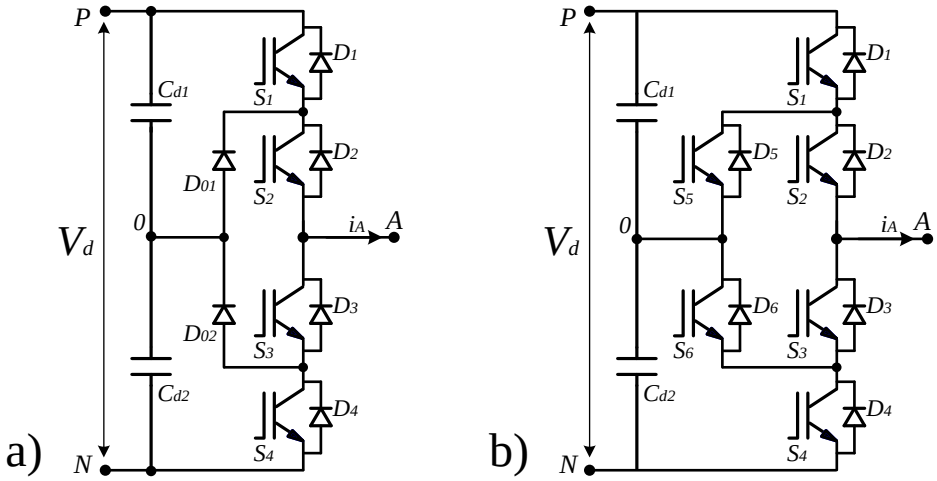


Figure 2.2. Illustration of one phase of a diode neutral point-clamped converter a), and one phase of an active neutral point-clamped converter b).

Cascaded H-Bridge

The cascaded H-bridge converter was created to obtain high output voltage from some lower voltage sources [12]. To achieve this goal some single-phase H-bridge power cells (like the cell shown in Figure 2.3) per phase are connected in cascade on their AC side. Each cell is fed by an isolated DC voltage (*E*), which can be achieved by independent DC sources, or through a multi-pulse transformer and as many rectifiers as cells there are in the converter. In this way the converter looks like is shown in Figure 2.4.

In those conditions, the output voltage of each one of the phases in the converter is calculated as the sum of the individual voltages of all the cells that compose a phase, having as a resultant voltage a signal with as many levels as twice the number of cells in a phase plus one ($2 \cdot Num.\ of\ cells + 1$). In the same line, the maximum and minimum voltage that a phase can reach is as many times the voltage supply (*E*) as the number of H-bridges in a phase ($\pm E \cdot Num.\ of\ cells$).

Moreover, this topology has an important advantage: the modularity. This means that if one device fails, it only affects to its cell, and the rest of the converter is able to keep working, meanwhile in other topologies, such as DNPC or ANPC, a fault in a device affects the whole converter.

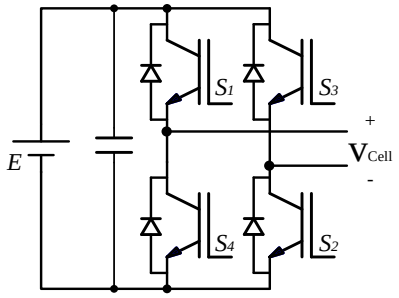


Figure 2.3. Single-phase H-bridge cell.

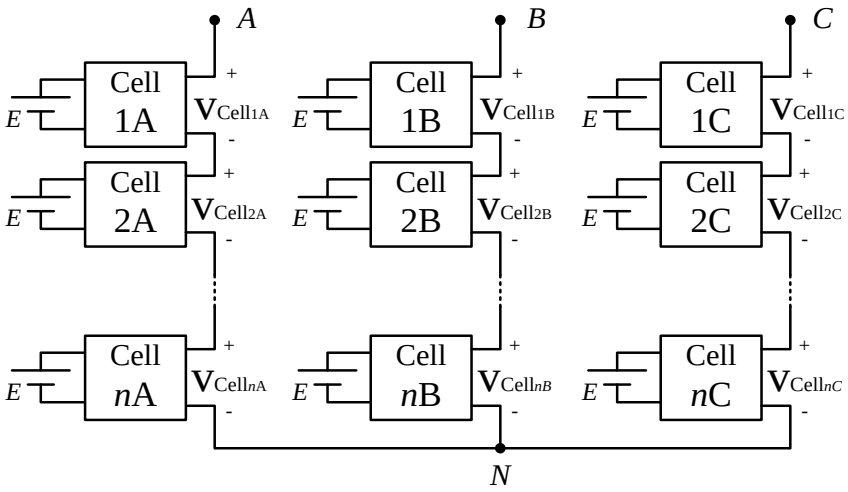


Figure 2.4. Example of a Cascaded H-Bridge converter with n cells per phase.

Modular Multilevel Converter

Modular Multilevel Converter (MMC) is composed by some submodules connected in series per phase achieving a great number of voltage levels [13]. The philosophy is similar to the cascaded H-bridge converter, but in this case there is a single DC supply. The basic submodule more used is a half-bridge, like the shown in Figure 2.5. It consists of two active devices (Top and Bottom) that have complementary behavior, and a capacitor. The submodule output voltage is the bottom device voltage.

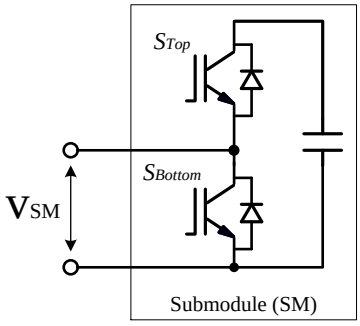


Figure 2.5. 2-Level SubModule (SM)

In this way, each phase of the converter is composed by *n* submodules that are spread evenly in two arms: the upper and the lower. Obviously to fulfil the above condition *n* must be an even integer.

Having *n* submodules per phase the number of levels that can be reached in the phase-to-neutral voltage is equal to $n/2 + 1$. Figure 2.6 shows an example of three-phase MMC with *n* submodules per phase. Following the nomenclature that appears in that figure, the phase-to-neutral voltage can be calculated from the expression:

$$V_{XN} = {}^{1}/_{2}\left[\left(v_{SM\,X1} + \cdots + v_{SM\,X(n/2)}\right) - \left(v_{SM\,X(n/2+1)} + \cdots + v_{SM\,Xn}\right)\right] \quad (2.1)$$

(being $X = A, B, C$; and n = total number of submodules in a phase)

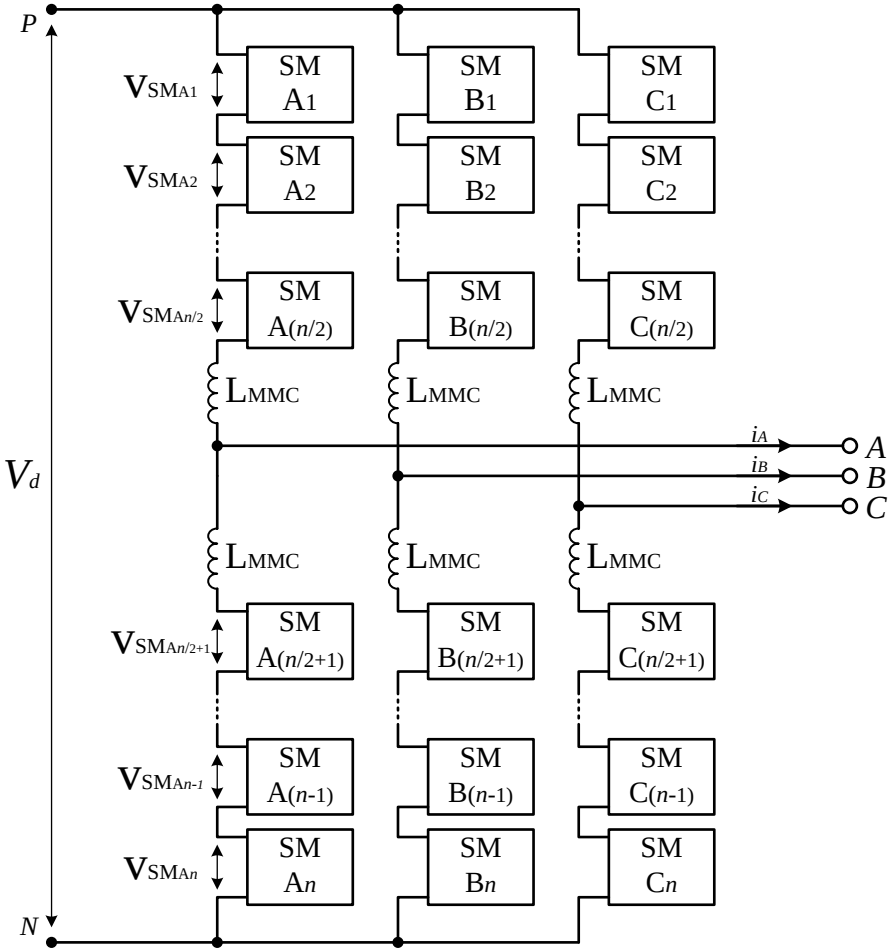


Figure 2.6. Modular multilevel converter with n submodules per phase

In this work the mentioned topologies are studied and compared one with each other, as they are four of the most used multilevel topologies in our days, and although there are some works studying these topologies separately, there is a lack of studies that relates all of them.

2.1.2. Modulation techniques background

The modulation method used to control a power converter is an important issue as it influences in the characteristics of the converter output signals. There are many modulation methods that can be applied to power converters, but for each topology some considerations should be met.

Figure 2.7 shows a classification of the most used modulation methods for multilevel converters. Mainly these methods are divided in two groups: those that use carrier signals, and those that do not. Probably the first group is the most used for neutral point-clamped

topologies and also for the multilevel topologies when they do not have a very high number of modules.

Those in the first group are commonly known as sinusoidal pulse-width modulation (SPWM), and they are based on the same principia: the comparison of a modulation reference signal with a set of carrier signals that usually have triangular shape [14]. The differences between these methods in the first group are related precisely with the carrier signals. These signals can be level-shifted that is the most commonly used for NPC topologies [15]-[17], or phase-shifted that is the best option for modular topologies [18]-[20]. Within the level-shift SPWM there are three options depending on how the carrier signals phases are interleaved: in-phase disposition (IPD), alternate phase opposite disposition (APOD), or phase opposite disposition (POD).

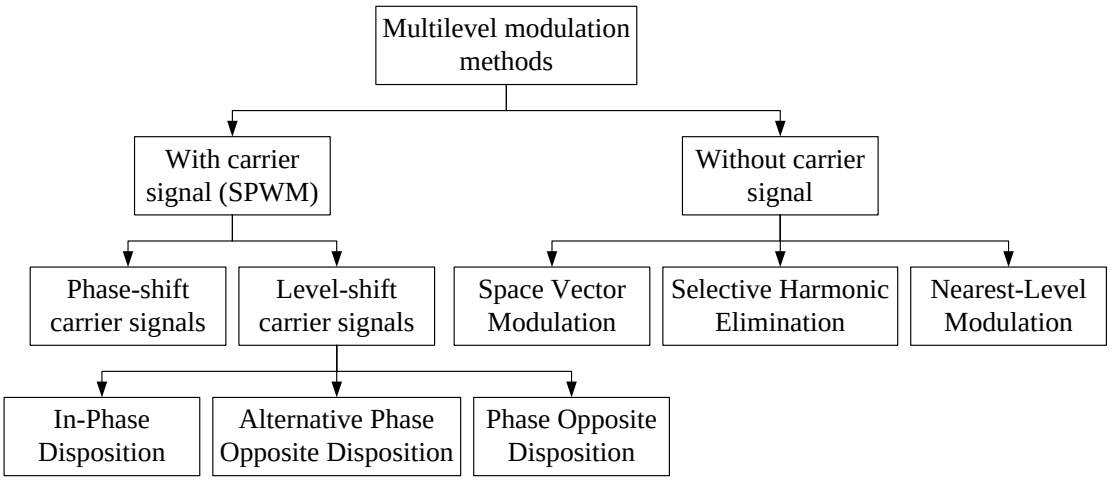


Figure 2.7. Classification of the main modulation methods used in power multilevel converters.

In the group of modulation techniques that do not use carrier signals are found the space vector modulation (SVM), the selective harmonic elimination (SHE), and the nearest-level modulation (NLM).

In SVM the voltage reference is represented as a vector that moves in a hexagonal space composed by all the possible switching states of the converter in which this method is applied. So, it is a modulation technique that can be applied in all converter topologies with only having in consideration that as high is the number of levels of the converter, as complex became the modulation method. This modulation technique has been used to control neutral point clamped converters [21], [22], and modular converters [23]-[25].

Nearest level modulation (NLM) is a modulation technique with simple principia. It consists on apply the converter voltage level that is closest to the reference voltage in each period of time [26], [27]. This technique is especially interesting to use in modular converters when the number of modules is very high and applying other techniques would imply a very high complexity.

On the other hand, selective harmonic elimination (SHE) is a modulation technique based on the off-line calculation of the optimal switching angles in order to eliminate certain harmonics in the output voltage. This technique was described for three-level converters as the neutral point-clamped topologies [28],[29], and after that, it has also been adapted to converters with more levels [30],[31].

In this line, in this Thesis work several sets of solutions for the 3-level SHE problem have been calculated with different number of eliminated harmonics. Also it has been calculated a solution of SHE for nine-level converters, and another set of angles to modulate six-level converters.

2.1.3. Fault-tolerant operation background

One of the principal concerns when a converter is designed, bought, or installed in an industry is the probability of faults occurrence, and if there is the possibility to keep the operation of that converter. The existence of this possibility is known as fault-tolerant operation.

In this line, the modular converters suppose an advantage over other kind of topologies as they allow in some cases the isolation of the faulty module or modules and the continuation of the operation, although it is not in the ideal conditions.

Concerning to cascaded H-bridge converters, there are many examples in the literature of fault-tolerant operation for maintaining the output phase-to-phase voltages balanced. The most simple for their implementation are bypassing the faulty cell and also the corresponding cells of the same level in the other phases; or also using converters with redundant H-bridges or redundant branches [32], [33]. The first solution has as drawback the voltage capacity loss, and the second one requires of the installation of extra cells, what increases the cost.

According to that the optimal solution is to bypass only the faulty cell or cells and act over the modulation in order to obtain balanced voltages. This can be done through the SVM using redundant states [34], [35], or modifying the voltage references of the three phases that is known as neutral-shift method [36], [37].

In this line, in this work an analytical neutral-shift method is proposed that can be directly implemented in simulation models, and with a few simplifications that will be explained, it can be also implemented in hardware control platforms.

Regarding to the modular multilevel converter, the philosophy is a little different when a fault occur in a submodule. In this case, as there is a single DC supply, the voltage is distributed between the non-faulty submodules, but the output voltage in the phase where there is a faulty submodule has less number of levels, and this fact get worse the currents quality.

Trying to solve this issue, there are publications like [38] that suggest the use of redundant submodules, but as in the case of CHB, this technique increase the final cost of the converter.

In this work what is done in order to minimize the THD increment in the case of faulty submodule is to rearrange the carrier signals in order to adapt their number to the number of the remaining 'sane' submodules in the phase.

2.2. Summary of contributions

As was mentioned in the first chapter, the main contribution of this work is to do an extensive comparative study of some of the most important multilevel topologies in our days. Although there was some studies about this field as [39]-[41], none of them relate the four chosen topologies in order to compare them. In other words, there is a lack of studies that compare the characteristics of traditional multilevel converters (3-levels) with the new modular topologies that can reach much more levels.

Within the study of modulation techniques for those topologies, special attention will be paid to the selective harmonic elimination, proposing several solutions for three-levels, six-levels, and nine-levels converters. Specifically in the case of applying SHE to active neutral point-clamped converters, an alternative proposal to choose the zero states is done in order to distribute equally the losses between the devices in the upper and lower halves of each phase.

Regarding to the operation under fault condition, an analytical neutral-shift method is proposed for controlling the cascaded H-bridge converter when there is a fault in a device. This method is designed in order to supply the maximum available balanced voltage in case of fault.

The studied topologies and modulation methods will be compared and also their usual medium voltage applications, that will do in order to do a proposal of which converter is more suitable for each application. This proposal will be supported by simulations and experimental tests.

Chapter 3: NEUTRAL POINT-CLAMPED TOPOLOGIES: DNPC - ANPC

This chapter is about the three-level neutral point-clamped topologies, and it explains the two most used variants: diode neutral point-clamped and active neutral point-clamped. Both topologies are very similar in terms of its control and the applications in which they are used, the main different between them is that, as the active NPC has active devices clamped to the neutral point instead of diodes the current path can be chosen, and also the DC bus can manage higher voltages, as the active devices are able to handle higher voltages than diodes. Another advantage of the ANPC over the DNPC is that the neutral point voltage is assured to be half the DC bus, as one of the clamped devices is always activated during the zero states. Moreover, the unequal power losses among the switching devices in the DNPC that causes uneven distribution of the semiconductor-junction temperature, is solved using the ANPC, as this topology can control the power loss distribution through the active clamped devices.

In the following subsections these two topologies are described, and also the most used modulation methods to control them.

3.1. Topologies description

As it was mentioned in the previous chapter the neutral point-clamped converters employ clamping devices and also two series DC capacitors to generate AC voltage waveforms with three levels. If the clamping devices are diodes we talk about diode neutral point-clamped (DNPC) converter, and if there are active devices clamped to the neutral point, it is an active neutral point-clamped (ANPC) converter. The following subsections show the main differences between these topologies.

3.1.1. Diode NPC

The 3-level Diode Neutral Point Clamped (DNPC) converter that was firstly described in [9], is a three-phase three-level power converter composed by four switching devices and two clamped diodes in each branch as it is shown in Figure 3.1. In this case the switching devices used in the DNPC converter are IGBT's with their corresponding free-wheeling diodes: $S_1 - D_1$, $S_2 - D_2$, $S_3 - D_3$, and $S_4 - D_4$.

The output phase-to-neutral voltage of a converter branch depends on the state (On-Off) of its switching devices. For the DNPC converter there are three different switching states known as P, 0, and N. These states are shown in Table 3.1. According to that, the output voltage in each converter phase can have three different levels: V_d /2, 0, and $-V_d$ /2. Note that, in NPC topologies, the phase-to-neutral voltage of each phase (v_{x0}) is measured between the output of the phase (x = A, B, or C) and the neutral point of the DC bus.

Table 3.1. Switching states for a phase of the DNPC converter (being x = A, B, or C).

Switching state	S_{x1}	S_{x2}	S_{x3}	S_{x4}	Phase voltage (v_{x0})
P	On (1)	On (1)	Off (0)	Off (0)	$V_d/2$
0	Off (0)	On (1)	On (1)	Off (0)	0
N	Off (0)	Off (0)	On (1)	On (1)	$-V_d/2$

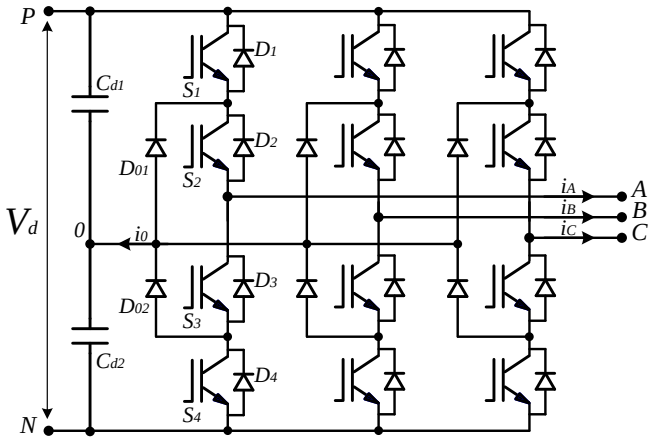


Figure 3.1. Diode Neutral Point Clamped converter with IGBT's.

3.1.2. Active NPC

The 3-level Active Neutral Point Clamped (ANPC) converter is an evolution of the diode neutral point clamped (DNPC) converter: ANPC (Figure 3.2) converters have active clamped devices to the neutral point instead of diodes ($S_5 - D_5$ and $S_6 - D_6$).

So, a 3-level ANPC converter is composed by six switching devices (IGBT's in this case) in each branch and their respective antiparallel diodes.

Due to the existence of active devices clamped to the neutral point, in the ANPC converters there are four different switching states to achieve the zero level in the output voltage. Therefore in this type of converters there are a total of six different switching states: V1 that represents V_d /2 voltage level; V2, V3, V4 and V5 that are the zero states; and V6 that represents the $-V_d$ /2 voltage level. Table 3.2 summarizes these states and the devices that are On or Off ('1' or '0') in each of them.

Table 3.2. Switching states for a phase of the active NPC converter (being *x* = A, B, or C).

Switching state	S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	S_{x6}	Phase voltage (v_{x0})
V_1	On (1)	On (1)	Off (0)	Off (0)	Off (0)	On (1)	$V_d/2$
V_2	Off (0)	On (1)	Off (0)	Off (0)	On (1)	Off (0)	0
V_3	Off (0)	On (1)	Off (0)	On (1)	On (1)	Off (0)	0
V_4	On (1)	Off (0)	On (1)	Off (0)	Off (0)	On (1)	0
V_5	Off (0)	Off (0)	On (1)	Off (0)	Off (0)	On (1)	0
V_6	Off (0)	Off (0)	On (1)	On (1)	On (1)	Off (0)	$-V_d/2$

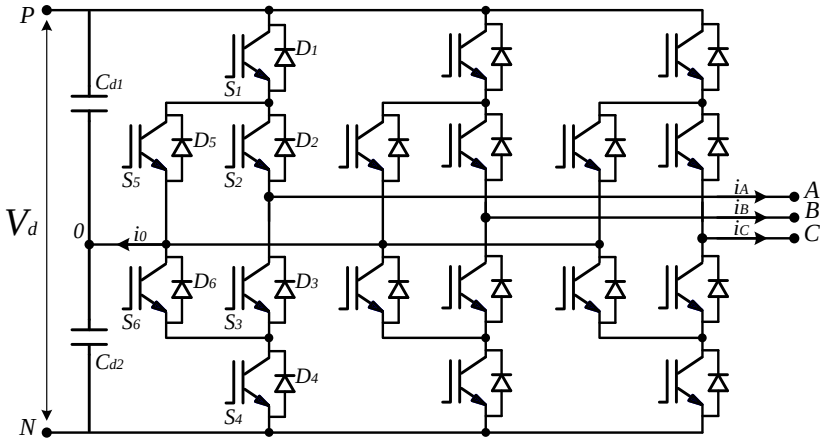


Figure 3.2. Active Neutral Point Clamped converter with IGBT's.

Depending on the sign of the output current the devices that conduce in each state are the IGBT's or the diodes. In Table 3.3 appear the conducting devices in each case.

Table 3.3. Conducting devices in each switching state

Switching state	Conducting devices	
	$I_x > 0$	$I_x < 0$
V_1	S_1, S_2	D_1, D_2
V_2	S_2, D_5	D_2, S_5
V_3	S_2, D_5	D_2, S_5
V_4	D_3, S_6	S_3, D_6
V_5	D_3, S_6	S_3, D_6
V_6	D_3, D_4	S_3, S_4

Moreover, the typical phase-to-neutral output voltage of a 3-level converter is as the shown in Figure 3.3. So, in the normal operation of the ANPC converter there are commutations between the $V_d/2$ voltage level and the zero level, and between the $-V_d/2$ voltage level and the zero level, that is the same as saying commutations between the states V1 or V6 and the zero states. These commutations between V1, V6 and the zero states, and the devices involved in them can be seen in Table 3.4.

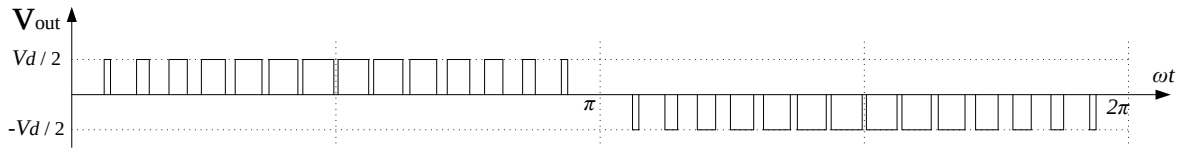


Figure 3.3. Typical phase-to-neutral output voltage in a 3-level converter.

As it is shown in Table 3.4, all commutations take place between one IGBT and one diode. Although more than two devices turn off, or on, only one active switch and one diode suffer significant switching losses. So, these commutations to, or from the zero states determine the distribution of the power losses among the converter devices. Hence the importance to choose the appropriate zero states in the switching strategies.

Table 3.4. Devices involved in the commutations between the different states of the ANPC converter.

	$I_x > 0$											
	S_1	D_1	S_2	D_2	S_3	D_3	S_4	D_4	S_5	D_5	S_6	D_6
$V_1 \leftrightarrow V_2$	√									√		
$V_1 \leftrightarrow V_3$	√									√		
$V_1 \leftrightarrow V_4$			√			√						
$V_1 \leftrightarrow V_5$	√					√						
$V_6 \leftrightarrow V_2$			√					√				
$V_6 \leftrightarrow V_3$			√			√						
$V_6 \leftrightarrow V_4$								√			√	
$V_6 \leftrightarrow V_5$								√			√	
	$I_x < 0$											
	S_1	D_1	S_2	D_2	S_3	D_3	S_4	D_4	S_5	D_5	S_6	D_6
$V_1 \leftrightarrow V_2$		√							√			
$V_1 \leftrightarrow V_3$		√							√			
$V_1 \leftrightarrow V_4$				√	√							
$V_1 \leftrightarrow V_5$		√			√							
$V_6 \leftrightarrow V_2$				√			√					
$V_6 \leftrightarrow V_3$				√	√							
$V_6 \leftrightarrow V_4$							√					√
$V_6 \leftrightarrow V_5$							√					√

So, the main difference between both topologies is the path that the current follows during the zero state: in case of DNPC the current path will be fixed by the own topology, and in ANPC the path can be chosen through modulation. In Figure 3.4 and Figure 3.5 one branch of each converter has been reproduced in order to illustrate the possible current paths.

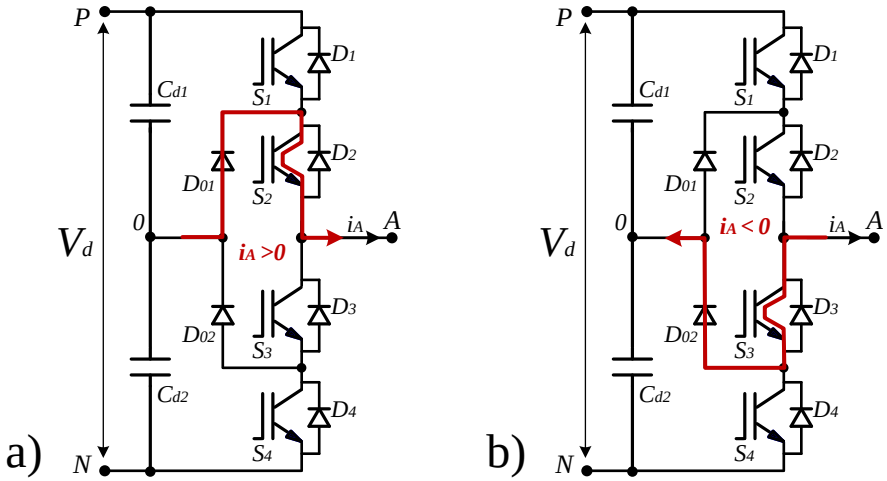


Figure 3.4. Current path in DNPC converter during zero state: when the output current is positive a), and when it is negative b).

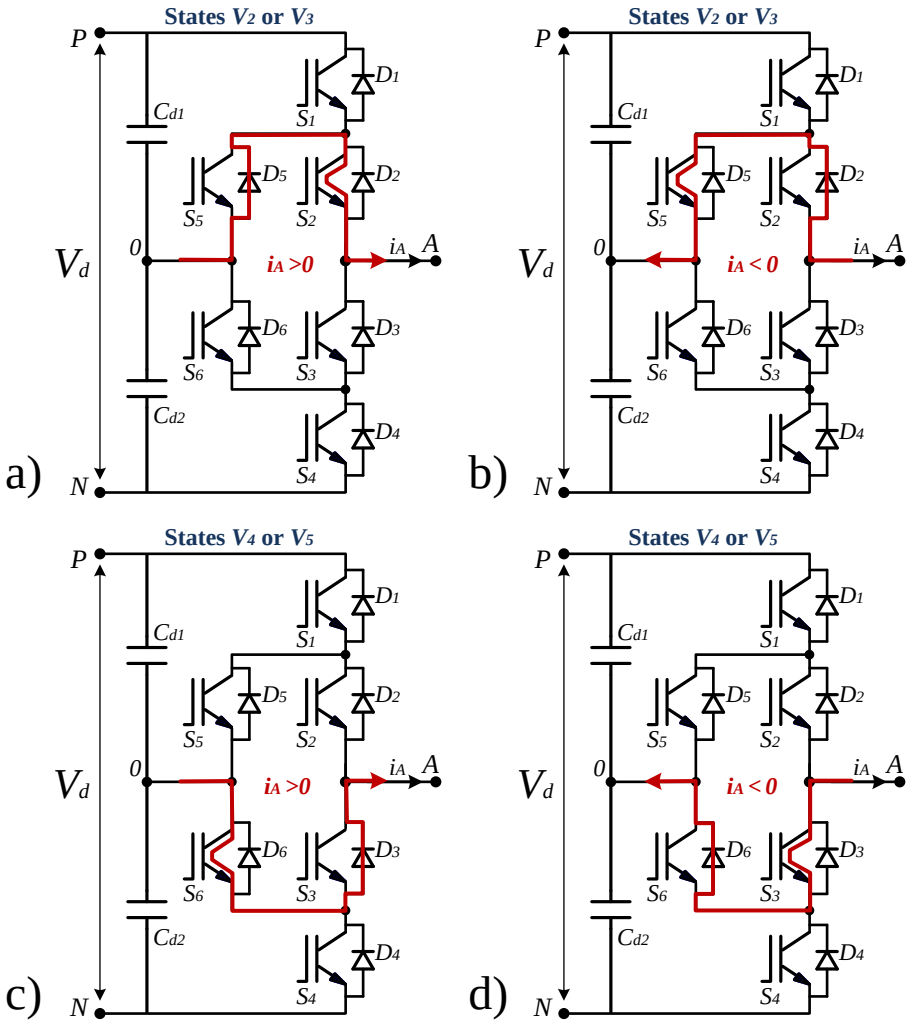


Figure 3.5. Current path in ANPC converter during zero state: when states V_2 or V_3 are applied and the output current is positive a), when those states are selected and the current is negative b), when V_4 or V_5 are applied with positive current c), and negative current d).

So, as it was mentioned, the zero states in the ANPC converter should be chosen carefully in order to avoid extra commutations and to distribute the losses equally among all the devices. In this line, the author proposed a new switching strategy in order to balance the ANPC switching losses [42] that will be explained in the following subsection.

3.2. Modulation methods

As both topologies are modulated in similar way, in this section the following methods used with both NPC converters will be explained in a general way:

- sinusoidal pulse-width modulation (SPWM)
- space vector modulation (SVM)
- selective harmonic elimination (SHE)

The only difference between both converters modulation is the zero state selection process for the ANPC that will be explained at the end of this subsection.

3.2.1. Sinusoidal Pulse-Width Modulation for NPC converters

Sinusoidal pulse-width modulation (SPWM) is probably the most used modulation scheme due to its simplicity and the ease of implementation. This modulation scheme is based in the comparison between three sinusoidal signals called modulation signals, with triangular signals with higher frequency than the previous ones that are known as carrier signals.

In the case of SPWM applied in three-phase NPC converter, there are three modulation signals (one per phase) shifted 120 degrees one from each other, and the most common is using two carrier signals level shifted that are compared with the modulation ones. The firing signals for the converter devices are obtained as follows:

$$v_{S_{1X}} = \overline{v_{S_{3X}}} = \begin{cases} 1 & if \ \ v_{mX} > v_{cr1} \\ 0 & else \end{cases}$$
$$v_{S_{2X}} = \overline{v_{S_{4X}}} = \begin{cases} 1 & if \ \ v_{mX} > v_{cr2} \\ 0 & else \end{cases} \qquad (3.1)$$
$$(\text{being } X = A, B, C)$$

where S_{1X}, S_{2X}, S_{3X}, and S_{4X}, are the devices in phase X, v_{mX} is the modulation signal for phase X, and v_{cr1} and v_{cr2} are the carrier signals for all phases. The firing signals generation process defined in (3.1) is represented in Figure 3.6 for phase *A*, and is similar for phases *B* and *C*.

In order to relate the modulation signal and the carrier signals amplitudes, the amplitude modulation index is defined (m_a). This variable is generally calculated as the quotient between the modulation signal amplitude divided by the carrier signal amplitude. This is in general terms, but in this case, as there are two carrier signals with half of the amplitude, m_a is calculated as the relation between the modulation signal amplitude and twice the amplitude of one carrier signal.

A generic triangular signal (v_{tri}) can be mathematically expressed as the arccosine of a cosine function with a specific frequency [45]:

$$v_{tri}(t) = v_{origin} + v_{amp}\left\{1 - \frac{2}{\pi}\text{acos}\left[-\cos\left(m_f \omega t + \varphi\right)\right]\right\} \tag{3.2}$$

where v_{origin} and v_{amp} are the signal origin and amplitude, respectively; m_f is the frequency modulation index defined as the relationship between the carrier signal and the modulation signal frequencies, ω is the fundamental pulsation, and φ is the angle shift between the modulation signal and the carrier signal. Equation (3.2) has been used to formulate the carrier signals in all the theoretical analysis of this Thesis.

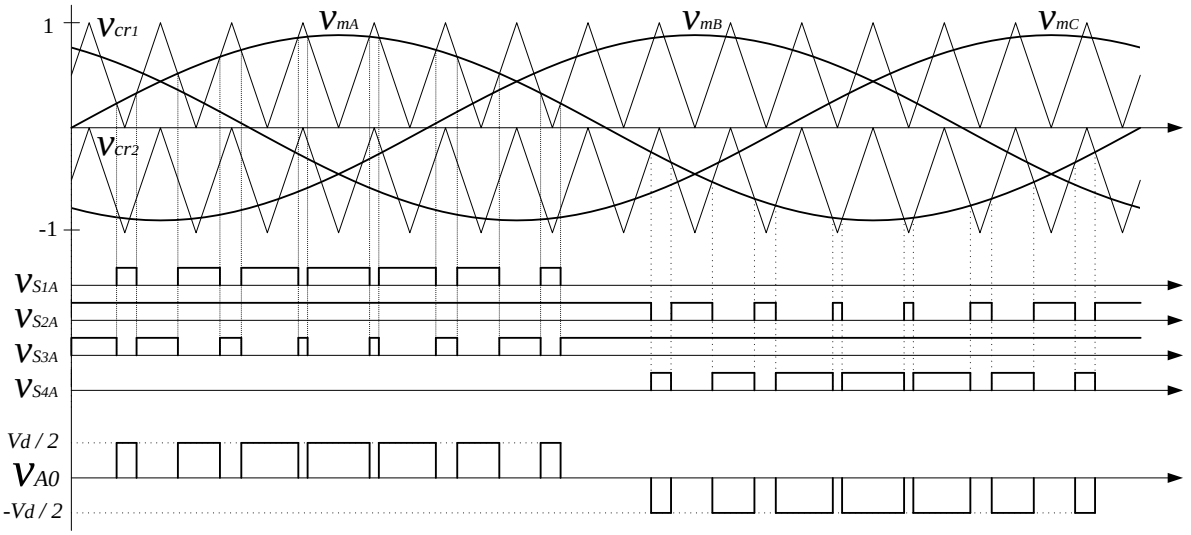


Figure 3.6. Example of Sinusoidal PWM for a DNPC (m_f = 15, m_a = 0.85).

Knowing that, the reader may see that in the example shown in Figure 3.6 the carrier signals, v_{cr1} and v_{cr2}, have amplitude of 1/2, their origins are 1/2 and -1/2 respectively, and its frequency is fifteen times higher than for the modulation signal. In Figure 3.6 both carrier signals have the same phase-shift (π/2 radians in this case) respect to the modulation signal, what is known as "in-phase disposition" (IPD), but they could have also different shift, in those cases one carrier is opposite to the other one, so this situation is known as "phase opposite disposition" (POD). The comparison between these two cases appears in Figure 3.7.

Both dispositions can be used for NPC converters with similar results. For example, Figure 3.8 shows the harmonic content of phase-to-neutral voltage of phase A when IPD and POD dispositions are used. As it can be seen, in both cases the main harmonic band appears around m_f, and a second lower band appears around $2m_f$. But seeing the harmonics disposition in detail some differences can be appreciated. In order to illustrate better those differences, in Figure 3.9 the harmonics belonging to the first and second bands have been represented versus de amplitude modulation index. It can be seen in Figure 3.9 that when the in-phase disposition is used, the first band is composed by odd harmonics and in the case of POD by even harmonics. The second band is integrated by odd harmonics in both cases.

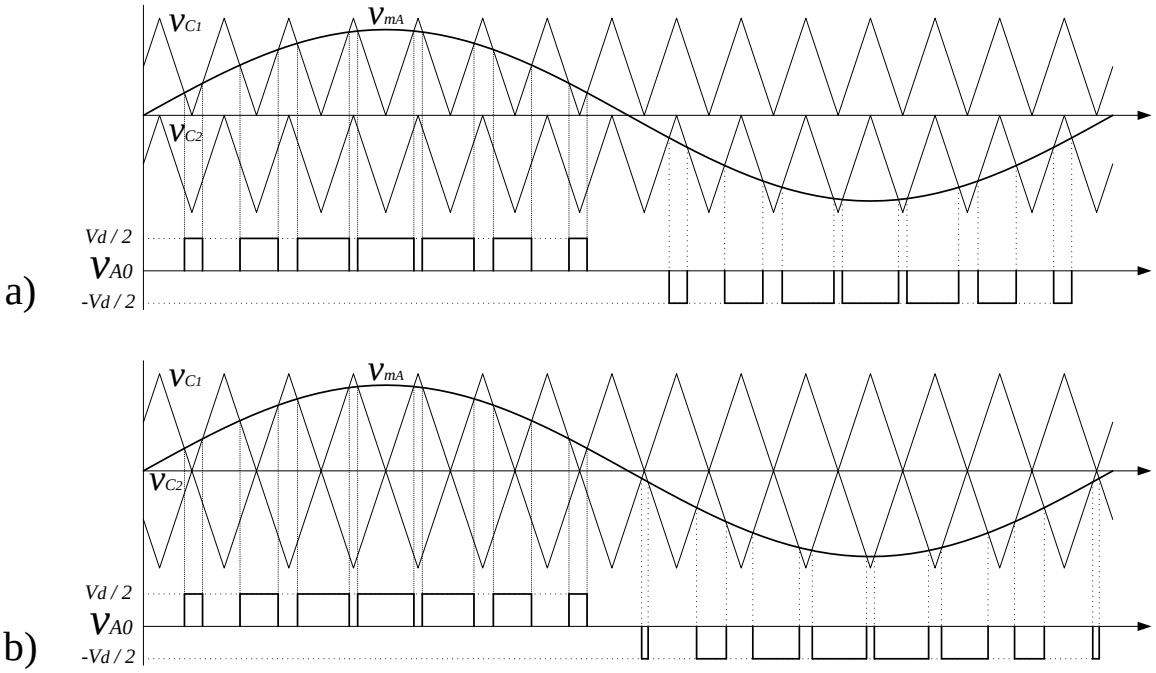


Figure 3.7. Example of carrier signals "in-phase disposition" - IPD a); and in "phase opposite disposition" - POD b). Both for m_f = 15 and m_a = 0.85.

The difference between the carrier dispositions may be seen also in the resultant voltage wave v_{A0} in Figure 3.7.a) and b): in the first case the signal has both quarter-wave symmetry and half-wave symmetry; meanwhile in the second case it has not any of them. Those little differences do not affect to the total harmonic distortion and the weight total harmonic distortion, as it can be seen in Figure 3.10.

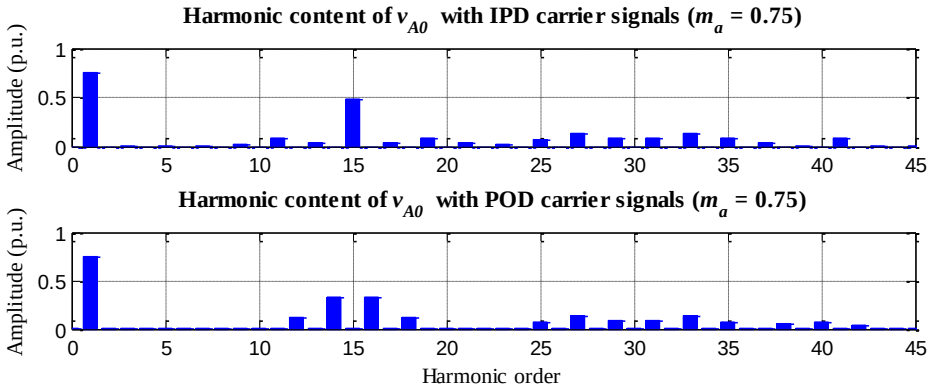


Figure 3.8. Harmonic content of phase-to-neutral voltage for an amplitude modulation index of 0.75 and m_f = 15 when IPD carrier signals are used a); and for POD signals b).

Turning to Figure 3.6, the reader can observe that the carrier signals have a phase-shift of $\pi/2$ radians with respect to the modulation signal, but they may not have any phase-shift. These two situations are illustrated in Figure 3.11.

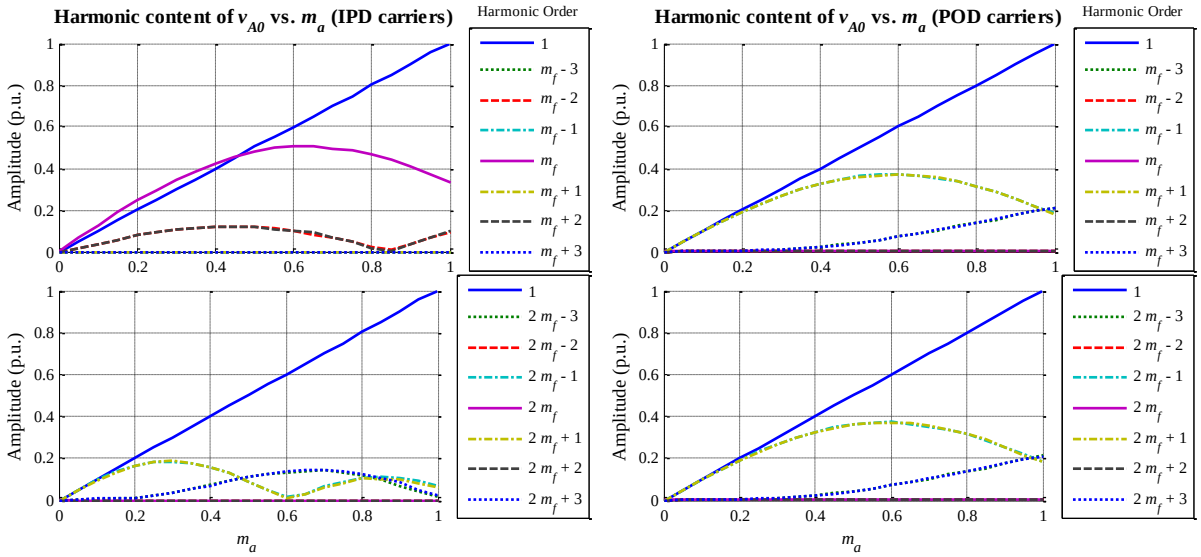


Figure 3.9. Harmonic content of the phase-to-neutral signal, v_{A0}, vs. m_a when IPD carrier signals are used a); and using POD signals b).

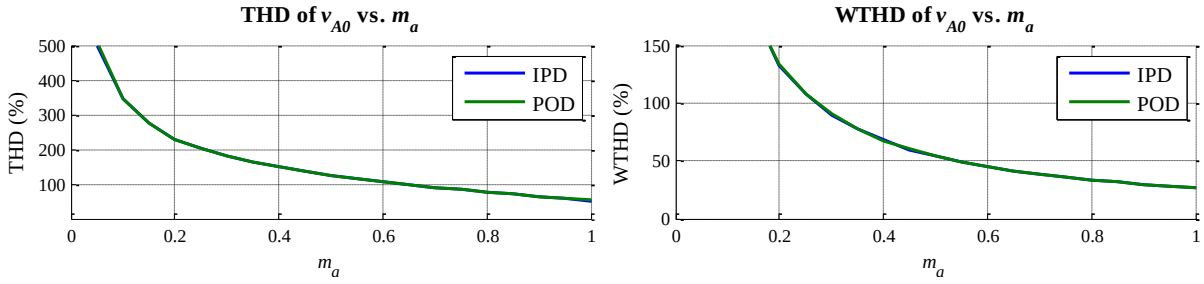


Figure 3.10. THD and WTHD of the phase-to-neutral voltage, v_{A0}, vs. m_a when IPD carrier signals are used a); and using POD signals b).

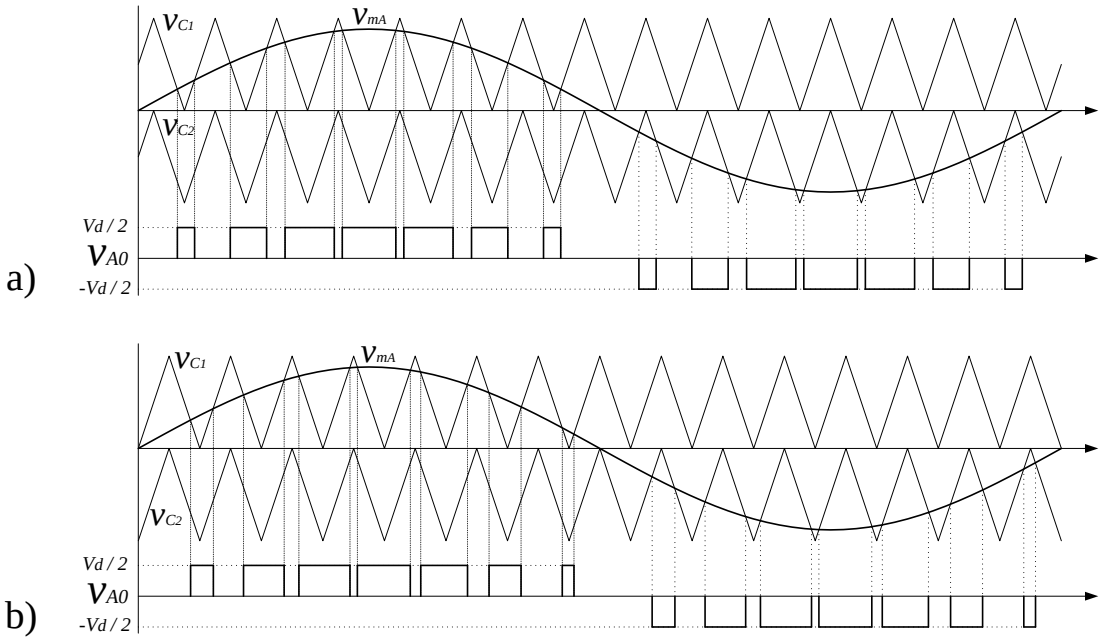


Figure 3.11. Example of carrier signals with phase-shift of π/2 radians a); and without phase-shift b). Both for m_f = 15 and m_a = 0.85.

As in the previous comparison of Figure 3.7, the two sets of carrier signals that appear in Figure 3.11 can be used with similar results, but little differences can be appreciated: in Figure 3.11.a) the resultant phase-to-neutral signal has quarter-wave symmetry, while the signal in Figure 3.11.b) is half-wave symmetry. Also the harmonic disposition in the second band is different (see Figure 3.12): when a phase shift of π/2 radians is used in the second band only odd harmonics appear; and if no phase shift is applied to the carrier signals the second band is composed by even harmonics. As happened in the previous comparison, these little differences do not affect to the total harmonic distortion (Figure 3.13).

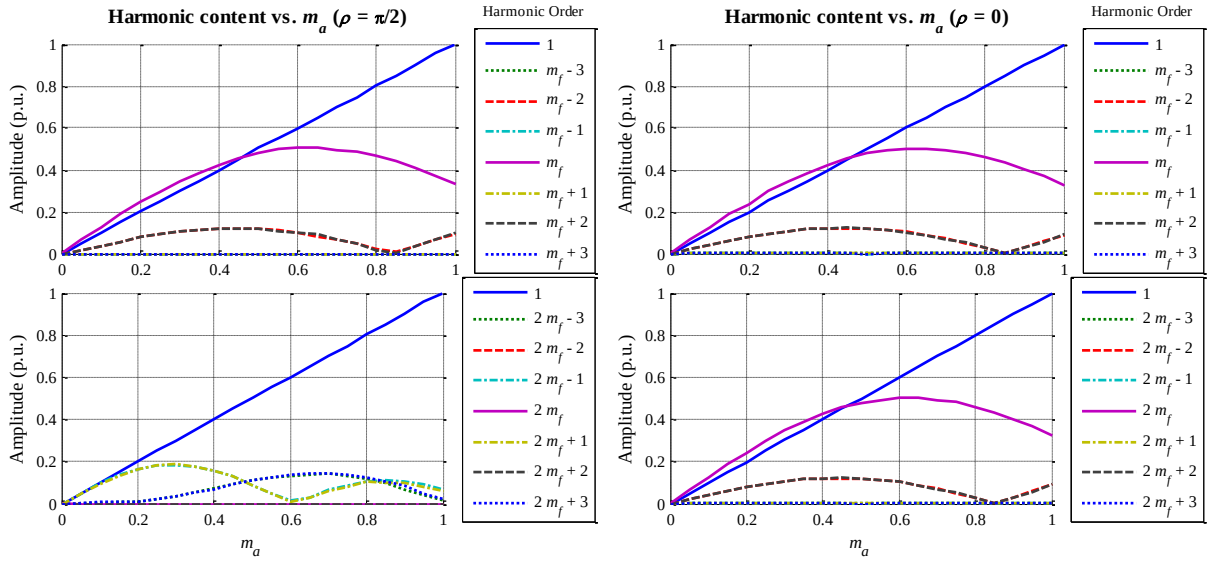


Figure 3.12. Harmonic content of the phase-to-neutral signal, v_{A0}, vs. m_a when carrier signals has $\varphi = \pi/2$ a); and when carrier signals has $\varphi = 0$ b).

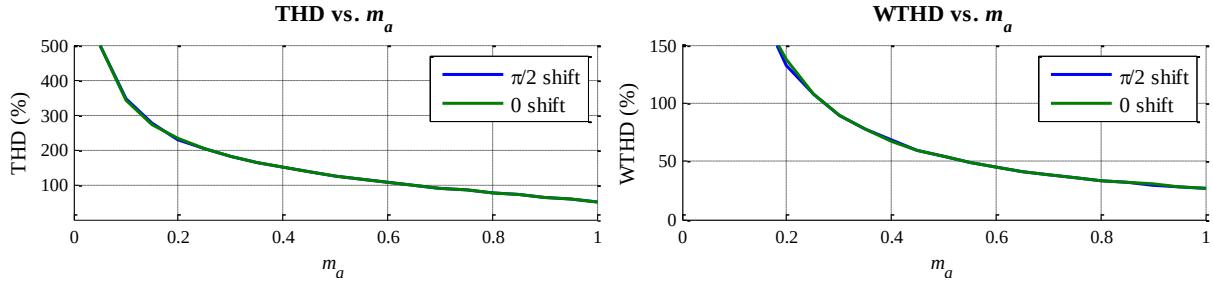


Figure 3.13. THD and WTHD of the phase-to-neutral voltage, v_{A0}, vs. m_a when carrier signals has $\varphi = \pi/2$ a); and when carrier signals has $\varphi = 0$ b).

In this work the chosen disposition for the carrier signals is the shown in Figure 3.7.a): in-phase disposition and $\varphi = \pi/2$, because it generates phase-to-neutral voltages with quarter-wave symmetry.

The reader should note that a similar analysis could be done for the phase-to-phase voltages, being the differences similar but less appreciable. In the case of the phase-to-phase voltages, the first band of harmonics will appear around $2m_f$.

3.2.2. Space Vector Modulation for NPC converters

Space Vector Modulation (SVM) is a very well-known modulation method used to control power converters. In the case of use this method in a three-phase three-level converter the possible switching states are a total of 27 (3^3). The 27 switching states are represented by 19 voltage vectors, what means that some of the states are redundant, or what is the same to say that some states correspond to the same voltage vector. Table 3.5 summarizes the relationship between the switching states and the voltage vectors in a NPC converter, where '*P*', '*O*', and '*N*' represent respectively the voltage levels $V_d/2$, 0, and $-V_d/2$.

Table 3.5. Switching states related to their corresponding voltage vectors for a neutral point-clamped converter.

Space Vector	Switching State		Vector Group	Module
$\vec{V}_0$	[*PPP*], [*OOO*], [*NNN*]		Zero Vector	0
	Type P	***Type N***	Short Vectors	$\frac{1}{3}V_d$
$\vec{V}_1$	[*POO*]	[*ONN*]		
$\vec{V}_2$	[*PPO*]	[*OON*]		
$\vec{V}_3$	[*OPO*]	[*NON*]		
$\vec{V}_4$	[*OPP*]	[*NOO*]		
$\vec{V}_5$	[*OOP*]	[*NNO*]		
$\vec{V}_6$	[*POP*]	[*ONO*]		
$\vec{V}_7$	[*PON*]		Medium Vectors	$\frac{\sqrt{3}}{3}V_d$
$\vec{V}_8$	[*OPN*]			
$\vec{V}_9$	[*NPO*]			
$\vec{V}_{10}$	[*NOP*]			
$\vec{V}_{11}$	[*ONP*]			
$\vec{V}_{12}$	[*PNO*]			
$\vec{V}_{13}$	[*PNN*]		Large Vectors	$\frac{2}{3}V_d$
$\vec{V}_{14}$	[*PPN*]			
$\vec{V}_{15}$	[*NPN*]			
$\vec{V}_{16}$	[*NPP*]			
$\vec{V}_{17}$	[*NNP*]			
$\vec{V}_{18}$	[*PNP*]			

Figure 3.14 represents the switching states and the voltage vectors that describe the SVM for a three-level converter. As it can be seen in Figure 3.14 and Table 3.5, attending to their module, the voltage vectors can be classified into four groups:

- **Zero vector** ($\vec{V}_0$). It represents the three switching states in which the output voltage is zero ([*PPP*], [*OOO*], and [*NNN*]). The module of $\vec{V}_0$ is zero.

- **Short vectors** ($\vec{V}_1$ to $\vec{V}_6$). Their module is $V_d/3$. Each one of these vectors represents two switching states, one containing [*P*] and other containing [*N*]. For this reason they are classified as type P or type N.

- **Medium vectors** ($\vec{V}_7$ to $\vec{V}_{12}$). These vectors represent the states in which each one of the three phases in the converter has a different voltage level. The module of this vectors is $\sqrt{3}\,V_d/3$.

- **Large vectors** ($\vec{V}_{13}$ to $\vec{V}_{18}$). Their module is $2V_d/3$, and they represent switching states in which none of the phases are connected to the neutral point (*O*).

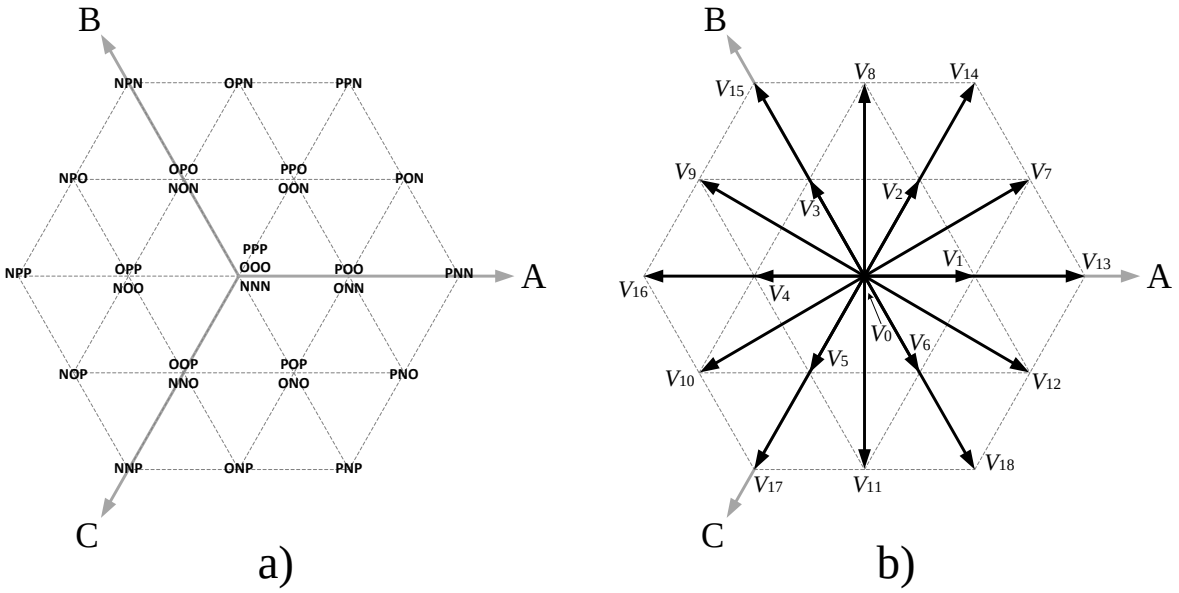


Figure 3.14. Switching states representation a), and voltage vectors b), in the space vector modulation for a three-level converter.

As shown in Figure 3.14, the space vectors divide the modulation hexagon in 24 triangles. Each one of those triangles is enclosed by the three voltage vectors that define its vertices. In this way, any voltage vector in the modulation hexagon can be expressed as a lineal combination of the three vectors that define the triangle where it lies. So, if a reference voltage vector lies in a triangle where the vertices are represented by $\vec{V}_a$, $\vec{V}_b$, and $\vec{V}_c$, the following statement is fulfilled:

$$\begin{aligned} \vec{V}_a T_a + \vec{V}_b T_b + \vec{V}_c T_c &= \vec{V}_{ref} T_s \\ T_a + T_b + T_c &= T_s \end{aligned} \tag{3.3}$$

Where T_s is the sampling period, and T_a, T_b, and T_c are the dwell times of vectors $\vec{V}_a$, $\vec{V}_b$, and $\vec{V}_c$ respectively.

Once the dwell times are calculated, the switching states represented by the corresponding vectors are applied during these periods respectively. When a vector represents redundant switching states, this operation should be done choosing with care the states in order to not introduce extra switching transitions when the reference vector moves from one triangle to another.

3.2.3. Selective Harmonic Elimination for NPC converters

Selective Harmonic Elimination was proposed in [28] for two and three levels inverters. This method consists on calculate "off-line" the angles in which switching events occur in order to eliminate a chosen number of harmonics near the fundamental one. These angles are used then to generate the switching events for the converter.

The shape of a generic three-level signal with quarter-wave symmetry is shown in Figure 3.15, where θ_1, θ_2, …, θ_N represent the angles in which switching events occur during a quarter of a period. So, in a period there are a total of $4N$ commutations in the signal.

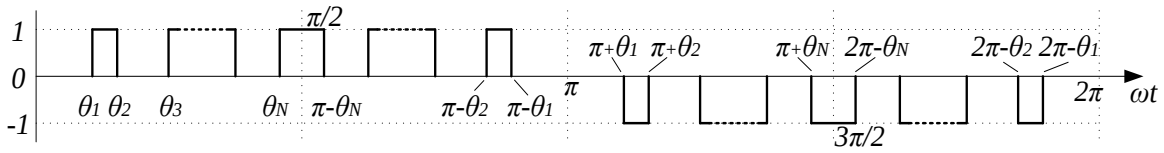


Figure 3.15. Generic three-levels wave with quarter-wave symmetry.

The angles' calculation is done using the Fourier series in order to decompose the three-level signal:

$$v_{out}(\omega t) = \sum_{n=1}^{\infty} [a_n \cdot \sin(n \cdot \omega t) + b_n \cdot \cos(n \cdot \omega t)] \tag{3.4}$$

where

$$\begin{cases} a_n = \dfrac{1}{\pi} \displaystyle\int_0^{2\pi} v_{out}(\omega t) \cdot \sin(n \cdot \omega t) \cdot d(\omega t) \\ b_n = \dfrac{1}{\pi} \displaystyle\int_0^{2\pi} v_{out}(\omega t) \cdot \cos(n \cdot \omega t) \cdot d(\omega t) \end{cases} \tag{3.5}$$

Assuming the quarter-wave symmetry, it is deduced:

- $a_n = 0$ for even harmonics (even n).
- $b_n = 0$ for odd and even harmonics (odd and even n).

As it can be observed, the symmetry (half-wave and quarter-wave) produces the even harmonics cancellation, so these harmonics have not been taken into account in the following process.

If the equation of a_n (3.5) is developed in the intervals between the switching events in the first quarter of the output signal, it is obtained for an odd number of events (odd *N*):

$$\begin{aligned} a_n &= \frac{4V_{dc}}{\pi}\left[\int_{\theta_1}^{\theta_2} \sin(n\cdot\omega t)\cdot d(\omega t) + \cdots + \int_{\theta_N}^{\pi/2} \sin(n\cdot\omega t)\cdot d(\omega t)\right] \\ &= \frac{4}{n\pi}\sum_{k=1}^{N}(-1)^{k+1}\cdot\cos(n\theta_k) \end{aligned} \tag{3.6}$$

And for an even number of switching events in the first quarter, it is obtained:

$$\begin{aligned} a_n &= \frac{4V_{dc}}{\pi}\left[\int_{\theta_1}^{\theta_2} \sin(n\cdot\omega t)\cdot d(\omega t) + \cdots + \int_{\theta_{N-1}}^{\theta_N} \sin(n\cdot\omega t)\cdot d(\omega t)\right] \\ &= \frac{4}{n\pi}\sum_{k=1}^{N}(-1)^{k+1}\cdot\cos(n\theta_k) \end{aligned} \tag{3.7}$$

From (3.6) and (3.7) it can be deduced that for any *N*:

$$a_n = \frac{4}{n\pi}\sum_{k=1}^{N}(-1)^{k+1}\cdot\cos(n\theta_k) \tag{3.8}$$

In this way, the amplitude of any harmonic, h_n, of the output signal can be expressed as a function of the *N* switching angles:

$$h_n = \frac{4}{n\pi}[\cos(n\theta_1) - \cos(n\theta_2) + \cdots + (-1)^{N+1}\cdot\cos(n\theta_N)] \tag{3.9}$$

Expressing the firsts *N* harmonics equations using the same procedure:

$$\begin{cases} f_1(\theta) = \cos(\theta_1) - \cos(\theta_2) + \cdots + (-1)^{N+1}\cdot\cos(\theta_N) = \dfrac{\pi h_1}{4V_{dc}} = \dfrac{\pi}{4}m \\ f_2(\theta) = \cos(3\theta_1) - \cos(3\theta_2) + \cdots + (-1)^{N+1}\cdot\cos(3\theta_N) = \dfrac{3\pi}{4V_{dc}}h_3 \\ \vdots \\ f_N(\theta) = \cos\big((2N-1)\theta_1\big) - \cdots + (-1)^{N+1}\cdot\cos\big((2N-1)\theta_N\big) = \dfrac{(2N-1)\pi}{4V_{dc}}h_{2N-1} \end{cases} \tag{3.10}$$

Using the set of equations (3.10) it is possible to eliminate the *N*-1 harmonics following the fundamental one, and to control the amplitude of first harmonic. This goal is achieved by setting to 0 the *N*-1 last equations and giving to the modulation index, *m*, a desired value:

$$\begin{cases} f_1(\theta) = \cos(\theta_1) - \cos(\theta_2) + \cdots + (-1)^{N+1} \cdot \cos(\theta_N) = \dfrac{\pi}{4} m \\ f_2(\theta) = \cos(3\theta_1) - \cos(3\theta_2) + \cdots + (-1)^{N+1} \cdot \cos(3\theta_N) = 0 \\ \vdots \\ f_N(\theta) = \cos\big((2N-1)\theta_1\big) - \cos\big((2N-1)\theta_2\big) \cdots + (-1)^{N+1} \cdot \cos\big((2N-1)\theta_N\big) = 0 \end{cases} \tag{3.11}$$

If the SHE is applied to a three-phase system, the triple harmonics are cancelled, so it is not necessary to calculate these harmonics. In such case the set of equations does not contain equations of any triple harmonic, and the last harmonic eliminated is 3*N*-1 if *N* is an even number, and 3*N*-2 if *N* is odd:

$$\begin{cases} f_1(\theta) = \cos(\theta_1) - \cos(\theta_2) + \cdots + (-1)^{N+1} \cdot \cos(\theta_N) = \dfrac{\pi}{4} m \\ f_2(\theta) = \cos(5\theta_1) - \cos(5\theta_2) + \cdots + (-1)^{N+1} \cdot \cos(5\theta_N) = 0 \\ f_3(\theta) = \cos(7\theta_1) - \cos(7\theta_2) + \cdots + (-1)^{N+1} \cdot \cos(7\theta_N) = 0 \\ \vdots \\ f_N(\theta) = \cos(X\theta_1) - \cos(X\theta_2) \cdots + (-1)^{N+1} \cdot \cos(X\theta_N) = 0 \end{cases} \tag{3.12}$$

$$X = \begin{cases} 3N-1 & for\ N\ even \\ 3N-2 & for\ N\ odd \end{cases}$$

Solving the equations system (3.12) with the desired value for *m* the first harmonic is controlled, and the following *N*-1 odd, non-triple harmonics are eliminated. The problem is that equations in (3.12) are non-linear and transcendental, what means that they cannot be solved through conventional methods. Usually to solve those equations approximation methods are used, like Newton-Raphson [28], genetic algorithms [43], etc. Also the resultant theory can be used [44] for this aim.

Figure 3.16 shows the angles sets obtained with the Newton-Raphson method for a three-phase three-level converter, with different number of events in a switching period: *N* from 3 to 11 angles. And in Figure 3.17 the phase-to-phase output harmonic content obtained with the different sets of angles has been represented. As the reader can see, for the same modulation index (in this case *m* = 0.8) the first harmonic that appears depends on the number of pulses contained in the used set (*N*).

As the number of calculated angles in the set determines the number of pulses in the output voltage (see Figure 3.15), this point has influence in the devices switching frequency. Table 3.6 summarizes the equivalence between the switching frequency with SHE and SPWM, and also relates the situation of the first harmonic following the fundamental that appears in the output phase-to-phase voltage. Note that for this comparison the fundamental frequency is taken as 50 Hz, and that in the case of ANPC converter the switching frequencies appeared in the table are valid for the active devices from S_1 to S_4, as the commutation of S_5 and S_6 depends on the zero state selection process.

Table 3.6. Equivalence between switching frequency in SHE and the SPWM modulation.

SHE			SPWM		
N	**Equivalent frequency**	**First harmonic**	m_f	**Switching frequency**	**First harmonic**
3	300 Hz	11th	7	350	14th (around)
4	400 Hz	13th	9	450	18th (around)
5	500 Hz	17th	11	550	22nd (around)
6	600 Hz	19th	13	650	26th (around)
7	700 Hz	23rd	15	750	30th (around)
8	800 Hz	25th	17	850	34th (around)
9	900 Hz	29th	19	950	38th (around)
10	1000 Hz	31st	21	1050	42nd (around)
11	1100 Hz	35th	23	1150	46th (around)

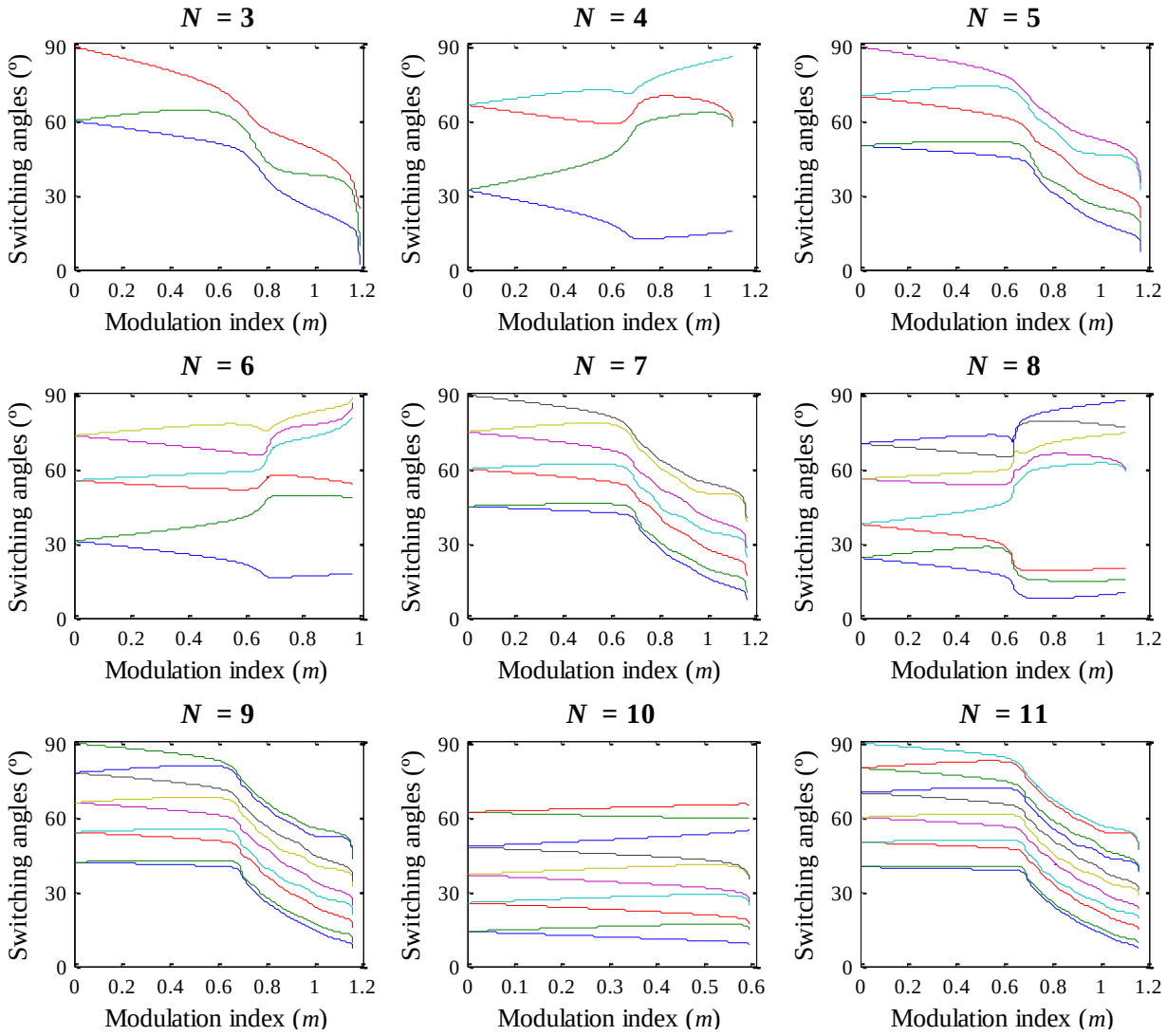


Figure 3.16. Switching angles vs. amplitude modulation index (m) for a three-phase three-level converter when N comes from 3 to 11.

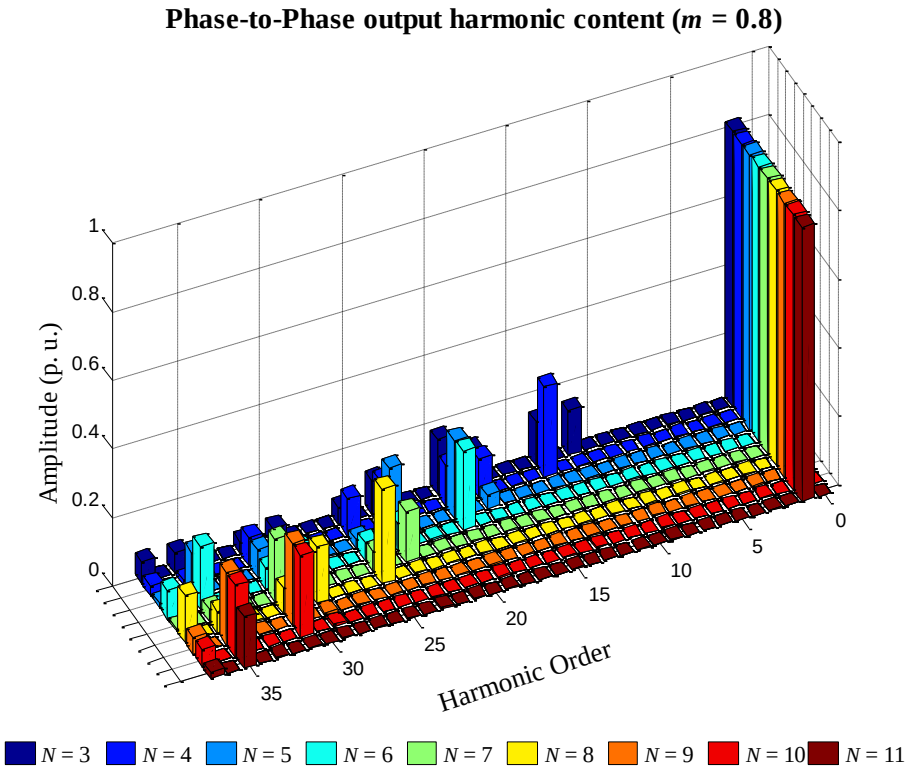


Figure 3.17. Phase-to-phase output harmonic content when the different sets of angles are used for the same modulation index (m = 0.8).

The implementation of selective harmonic elimination is very interesting for its applications in medium voltage converters working with very high power where the switching frequency should be very low. Moreover, combining this technique with high order grid filters that include a notch-type branch (like LLCL) gives the optimal solution to optimize the harmonic content of the currents that are supplied to the grid in this kind of applications.

3.2.3.1. Carrier-based selective harmonic elimination

Within the selective harmonic elimination technique there is a variant that consist on approximating a carrier-based scheme to the selective harmonic elimination. This approximation to a carrier-based scheme is interesting since a carrier-based modulation is easier to be included in closed loop applications than the traditional SHE. This technique was proposed in [45] for two-levels converters and it introduces a modification on the carrier signal equation (eq. (3.2)) in order to change the moment of the switching events and hence to achieve an output signal similar to that obtained with SHE method.

According to the previous, the carrier signals now are formulated generically as

$$v_{tri}(t) = v_{origin} + v_{amp}\left\{1 - \frac{2}{\pi}\text{acos}\left[-\cos\left(m_f \omega t + \beta(t) + \varphi\right)\right]\right\} \tag{3.13}$$

where v_{origin} and v_{tri} are the signal origin and amplitude, respectively; m_f is the frequency modulation index, ω is the fundamental pulsation, φ is the angle shift between the modulation signal and the carrier signal, and $\beta(t)$ is the modification function that allows the approximation between the carrier-based scheme and the SHE scheme.

The author of [45] uses for the carrier-based SHE scheme for two-level converter a modification function, $\beta(t)$, that depends on the fundamental frequency, the amplitude modulation index, and on a Bessel function of first kind.

However, in this work for adapting the carrier-based scheme to the SHE modulation, $\beta(t)$ has been calculated directly in order to create the two needed carrier signals for the NPC converters modulation, in such way that the output voltage is similar to that obtained with the SHE scheme. Specifically in this work it has been calculated a $\beta(t)$ to do the approximation to selective harmonic elimination with a set of seven angles (see the central plot in Figure 3.16). The direct calculation of this function is shown in Figure 3.18. Obviously the modification has only been calculated for a quarter of period, as the quarter-wave symmetry is respected also in this case.

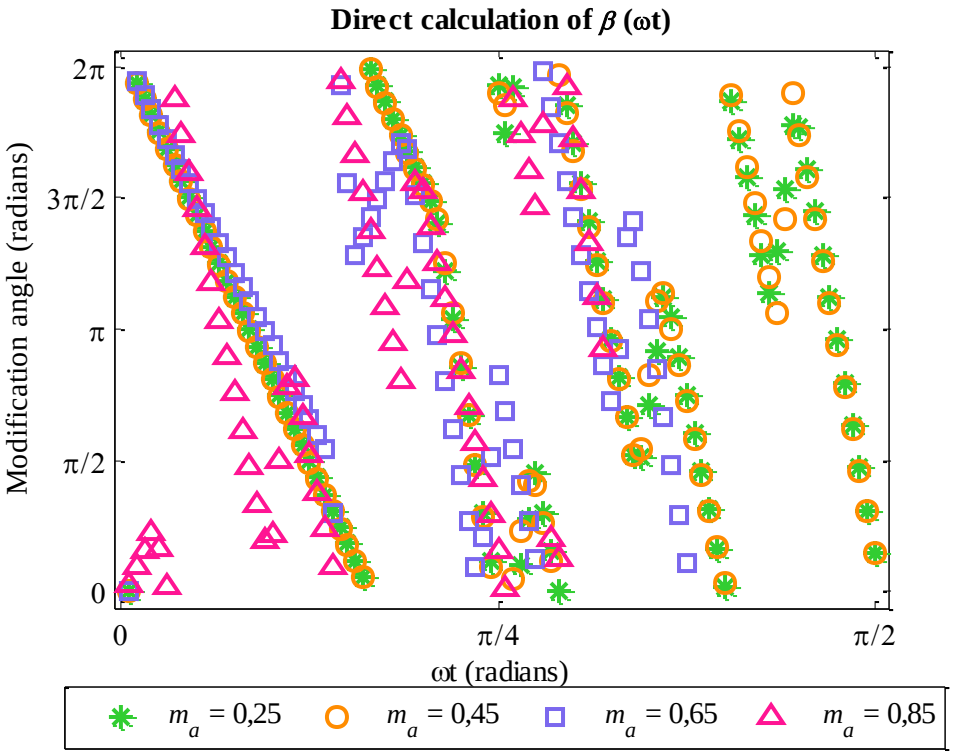


Figure 3.18. Direct calculation of the modification function, β(t), that is used to approximate the SHE scheme with carrier based modulation.

Figure 3.19 shows the resultant carrier signals after applying the modification function to the carrier signals equations. This figure contains four different examples for diverse modulation indexes. The figure also shows the output phase-to-neutral voltage (p.u.) obtained with this scheme, and it is compared with the same voltage generated with the SHE scheme. As the reader can see both signals in all cases are very similar, what means that with a carrier

based scheme is possible to obtain a harmonics spectrum that is similar to that obtained with the traditional scheme of selective harmonic elimination.

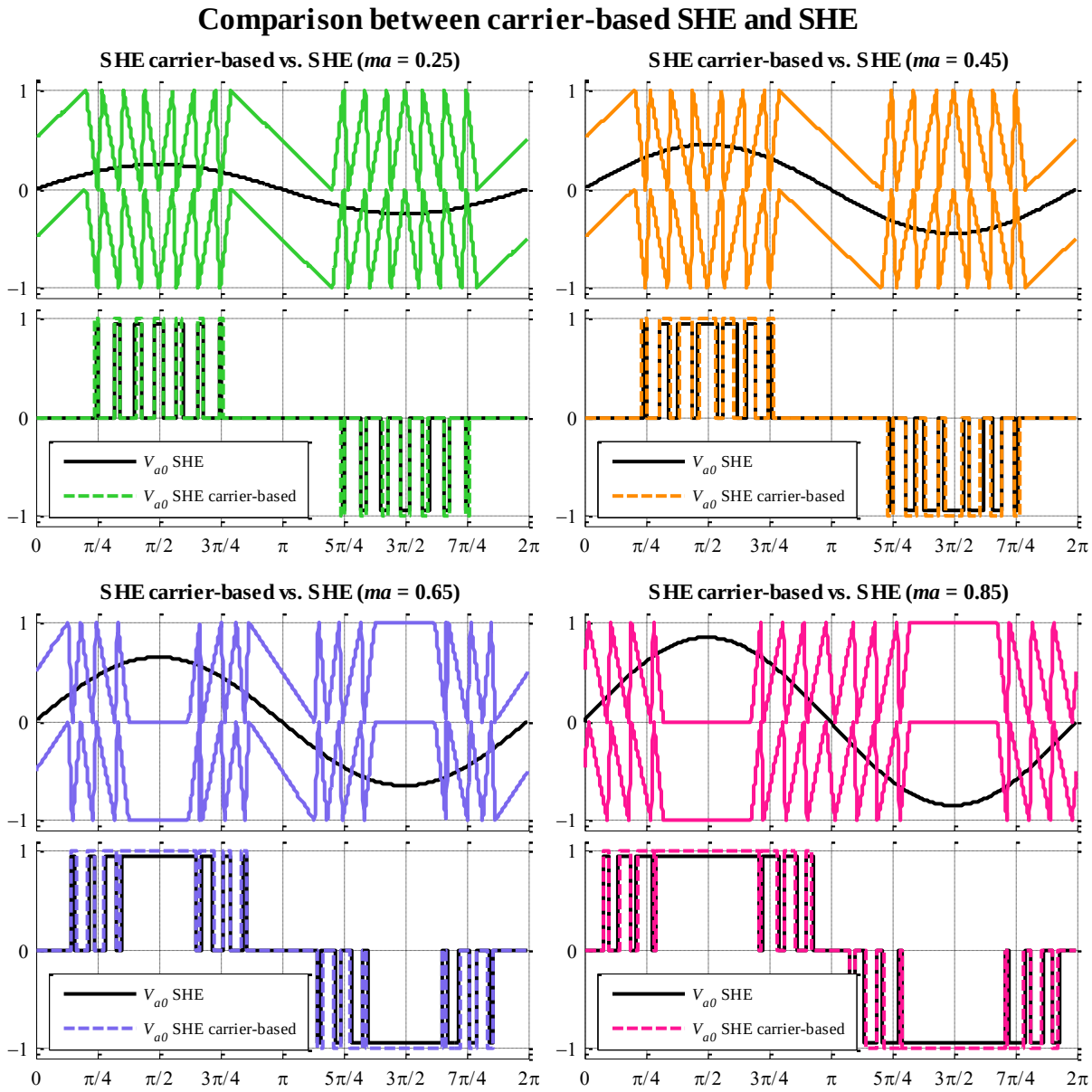


Figure 3.19. Examples of modified carrier signals calculated with the modification function for different modulation indexes, and phase-to-neutral signal (v_{a0}) obtained in each case.

3.2.4. Zero states switching selection

As was mentioned previously in this chapter, the selection of the zero state for the active neutral point-clamped converter is an important issue because it determines the current paths and hence, the switching and conduction losses.

There are many examples of techniques to choose the appropriate zero state [46]-[49]. Usually these techniques are independent from the used modulation method. Other times they depend on the modulation used, as is the case of [50] or [42], which are specific methods to

balancing the losses through the correct selection of the zero state when the SHE modulation is used. Specifically, in [42] is proposed an alternative method to improve the losses obtained with the method described in [50]. Both publications work with a set of seven angles (N = 7), [50] proposes the switching pattern shown in Figure 3.20. As it can be seen in that figure, in the interval 0-θ_1 is applied state V5, in interval θ_1-θ_2 is applied state V1, and so on.

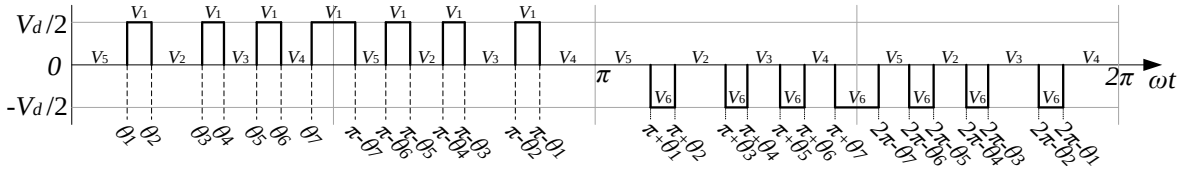


Figure 3.20. Switching strategy proposed in [50] for SHE modulation (N = 7).

From Figure 3.20, Table 3.3, and Table 3.4, the theoretical ANPC losses (p.u.) in a branch are calculated and summarized in Table 3.7. This table shows the losses in each pair IGBT-diode because both devices are usually in the same package. The conduction losses are expressed in the table as a function of the switching angles, and in Figure 3.21 they are also calculated theoretically for different modulation indexes.

Table 3.7. Per unit ANPC losses using switching strategy proposed in [50].

	Switching Losses	**Conduction Losses (*As a function of θ_1 to θ_7*)**
$S_1 - D_1$	11	$\pi - 2\theta_1 + 2\theta_2 - 2\theta_3 + 2\theta_4 - 2\theta_5 + 2\theta_6 - 2\theta_7$
$S_2 - D_2$	11	$\pi - 2\theta_1 - 2\theta_2 + 2\theta_3 - 2\theta_4 + 2\theta_5 + 2\theta_6 - 2\theta_7$
$S_3 - D_3$	10	$\pi + 2\theta_1 + 2\theta_2 - 2\theta_3 + 2\theta_4 - 2\theta_5 - 2\theta_6 + 2\theta_7$
$S_4 - D_4$	10	$\pi - 2\theta_1 + 2\theta_2 - 2\theta_3 + 2\theta_4 - 2\theta_5 + 2\theta_6 - 2\theta_7$
$S_5 - D_5$	8	$-4\theta_2 + 4\theta_3 - 4\theta_4 + 4\theta_5$
$S_6 - D_6$	6	$4\theta_1 - 4\theta_6 + 4\theta_7$

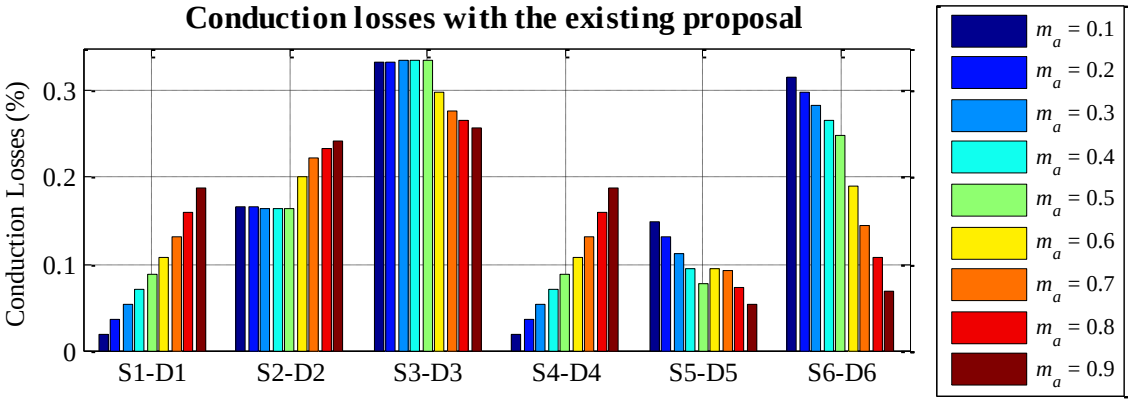


Figure 3.21. Theoretical conduction losses for the ANPC converter for different modulation indexes using switching pattern from [50].

From Figure 3.21 and Table 3.7 it can be seen that neither the switching nor the conduction losses are distributed homogeneously between all the devices in a branch whatever be the modulation index. This fact was expected since there are devices that lead the current in the V1 or V6 states, and also in some zero states. For example, it was expected that the conduction losses in the inner devices (i.e. the pair S-D_2) were higher than in the outer (i.e. the pair S-D_1), and this happens, but also it was expected that the conduction losses in both inner devices (S-D_2 and S-D_3) were almost equal, and this is not true. The losses are neither similar between the NPC devices (S-D_5 and S-D_6).

Seeing the ANPC configuration (Figure 3.2) and the devices experiment losses in each switching state (Table 3.3), it was expected that the losses was distributed almost equally between the pairs: S-D_1 and S-D_4, S-D_2 and S-D_3, and S-D_5 and S-D_6, so in [42] a new switching strategy is proposed and analyzed, which can be seen in Figure 3.22.

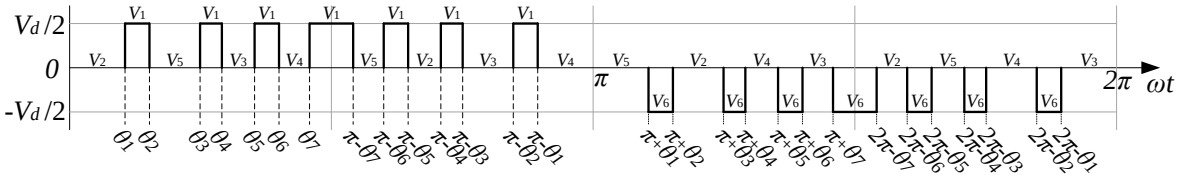


Figure 3.22. Switching strategy proposed in [42] for SHE modulation (N = 7).

Doing the same analysis than in the previous case, per unit losses are obtained and summarized in Table 3.8 and Figure 3.23. As it can be seen the calculated losses for the different modulation indexes are always distributed equally between the pairs: S-D_1 and S-D_4, S-D_2 and S-D_3, and S-D_5 and S-D_6, what is desirable in order to share the losses between the upper and the lower parts of each branch of the converter.

Note that, the theoretical analysis of the converter losses summarized in Table 3.7 and Table 3.8 have been made in an ANPC model, so they don't have into account the converter layout, neither the bus bars impedance. In an analysis for a real converter these parameters must be taken into account.

Table 3.8. Per unit ANPC losses using switching strategy proposed in [42].

	Switching Losses	**Conduction Losses (*As a function of θ_1 to θ_7*)**
$S_1 - D_1$	11	$\pi - 2\theta_1 + 2\theta_2 - 2\theta_3 + 2\theta_4 - 2\theta_5 + 2\theta_6 - 2\theta_7$
$S_2 - D_2$	10	π
$S_3 - D_3$	10	π
$S_4 - D_4$	11	$\pi - 2\theta_1 + 2\theta_2 - 2\theta_3 + 2\theta_4 - 2\theta_5 + 2\theta_6 - 2\theta_7$
$S_5 - D_5$	7	$2\theta_1 - 2\theta_2 + 2\theta_3 - 2\theta_4 + 2\theta_5 - 2\theta_6 + 2\theta_7$
$S_6 - D_6$	7	$2\theta_1 - 2\theta_2 + 2\theta_3 - 2\theta_4 + 2\theta_5 - 2\theta_6 + 2\theta_7$

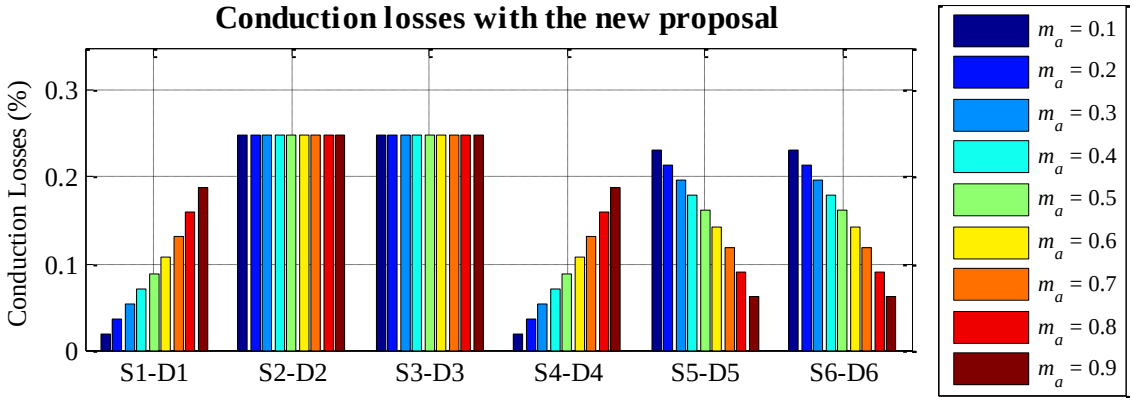


Figure 3.23. Theoretical conduction losses for the ANPC converter for different modulation indexes using switching pattern from [42].

3.3. Applications for NPC converters

In this section some typical applications for the neutral point-clamped topologies will be explained, including some examples of renewable energies connection, power quality applications (or commonly known as FACTS), and induction motor drives.

3.3.1. Distributed power generation

The renewable energies connection is an important subject nowadays because of the increase of this kind of energy resources. The neutral point-clamped topologies are very used for such purposes, but not always with the same configuration, what means that depending on the renewable resource the converter is connected in a different way.

For example, for the connection of photovoltaic solar panels to the grid it is very usual to use a NPC converter working as an inverter, as the photovoltaic panels generate DC power and the connection is done with an AC grid. This example is illustrated in Figure 3.24, and has been documented in many publications as [51]-[55].

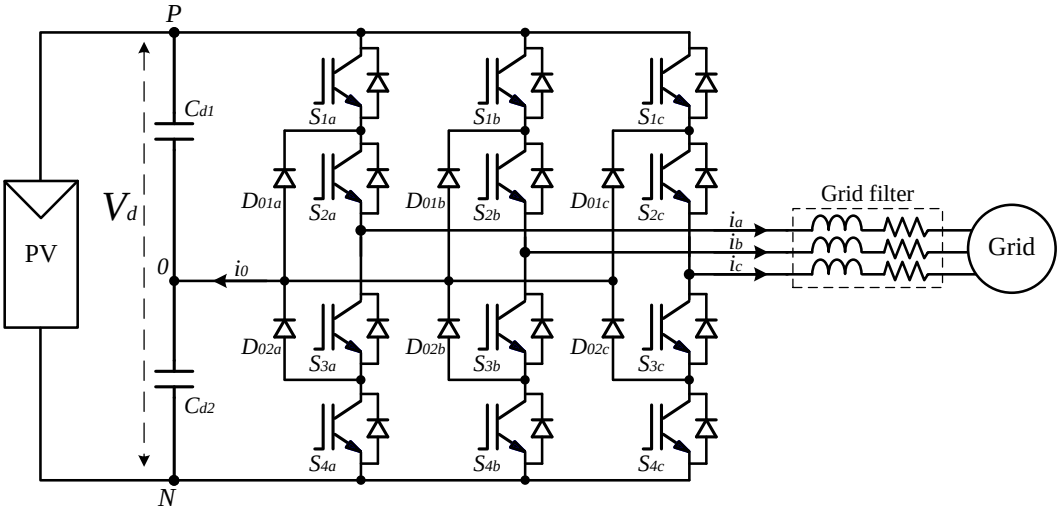


Figure 3.24. Example of PV panels connection with a distribution grid through a DNPC converter.

Another example of the integration of generated power coming from renewable resources with NPC converters is the connection of wind turbines. This connection can be done for both on-shore and off-shore wind turbines, and is usually done through a back-to-back configuration as is shown in Figure 3.25. There are many publications that describe this application of NPC converters: [56]-[59].

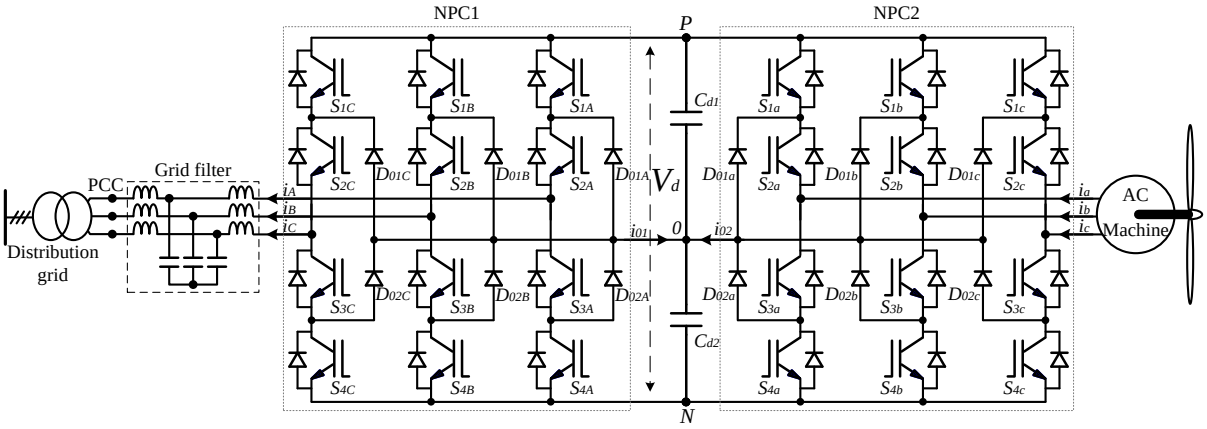


Figure 3.25. Example of wind turbine connection though DNPC converter with back-to-back configuration.

3.3.2. Power quality applications

The neutral point-clamped converters are also very used in power quality applications with the aim to improve de power quality. The grid-connected applications using NPC converters are diverse, such as active filters [60]-[61], Dynamic Voltage Restorers (DVR) [62], or reactive power compensators [63]-[65]. This last application, also known as static VAr compensators or STATCOMs, is a very common application that will be analyzed in detail in this work. The description and control basis of this application is explained in depth in Appendix B, but the reader can see in Figure 3.26 the basic scheme of a STATCOM system based in a DNPC converter.

3.3.3. Drive applications

The NPC topology is also very used for medium voltage induction motor drives, as is illustrated in the examples [66]-[69]. This application of the NPC converter also will be studied in detail later in this work, but the reader can see a basic illustration of this application in Figure 3.27. The operation and control of induction motors that will be used in this Thesis are described in Appendix C.

3.3.4. Peculiarities of neutral point-clamped topologies

It is worth to mention that, whatever be the application in which a neutral point-clamped converter is used, it is necessary to implement a controller for the neutral point voltage. The reason is that in the normal operation of a NPC converter the voltage in both DC

capacitors tends to become unbalance. If this unbalance between the capacitors voltages is not compensated, a DC component can appear in the output voltage. So, to avoid this effect it is very advisable to implement a neutral point voltage balancing method. There are some options to solve this problem depending on the used modulation methods: if it is used SVM redundant switching states can be applied for the same voltage reference; if the SHE scheme is used the balancing method described in [50] can be used; and for the SPWM modulation can be used the methods contained in [70] and [71]. Simplified blocks diagrams of the methods explained in [50], in [70] and in [71] appear in Figure 3.28, in Figure 3.29, and in Figure 3.30 respectively.

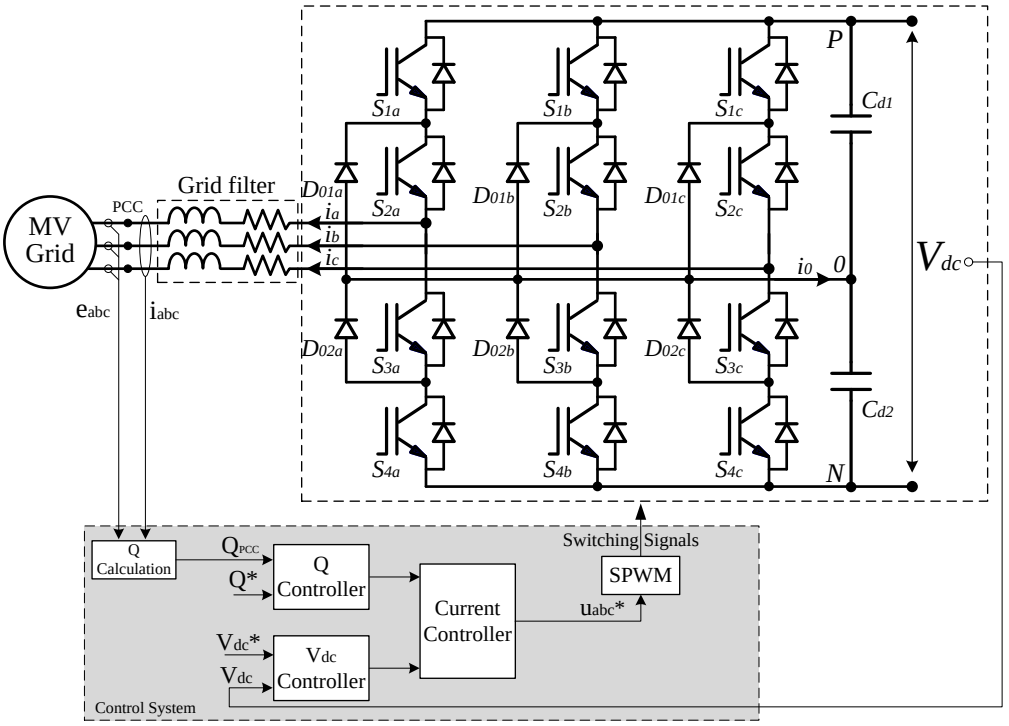


Figure 3.26. Basic scheme of a DNPC-based STATCOM.

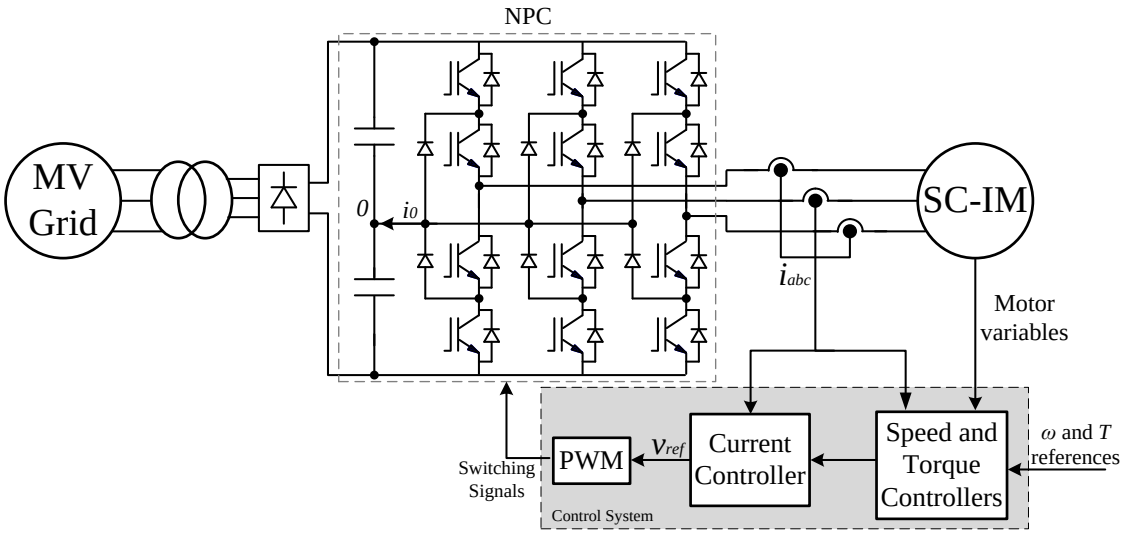


Figure 3.27. Illustration of a basic MV-drive with a DNPC converter.

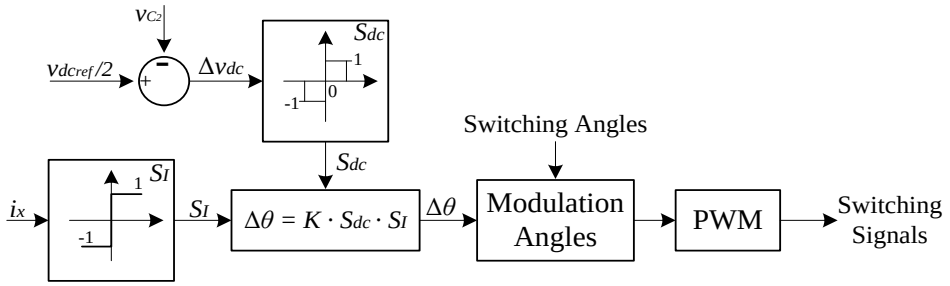


Figure 3.28. Block diagram of the neutral point voltage balancing method for SHE modulation explained in [50].

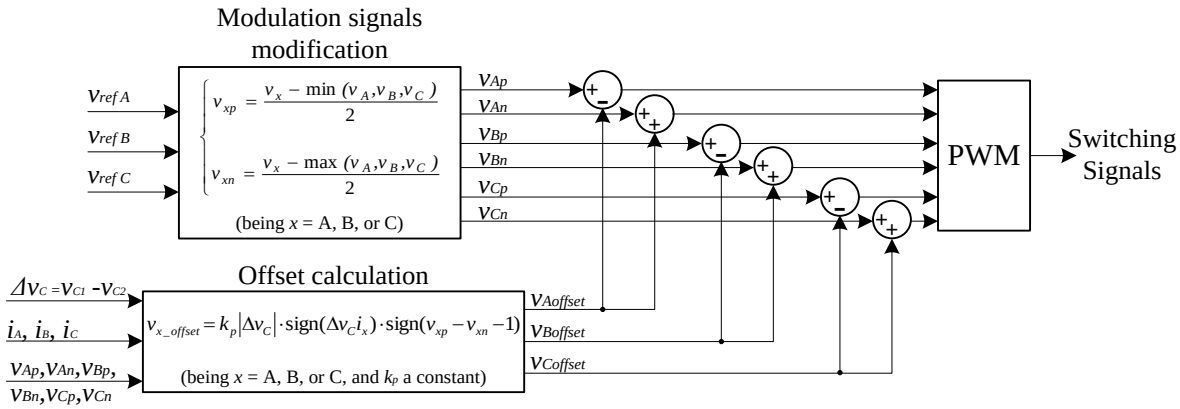


Figure 3.29. Block diagram of the neutral point voltage balancing method for SPWM modulation explained in [70].

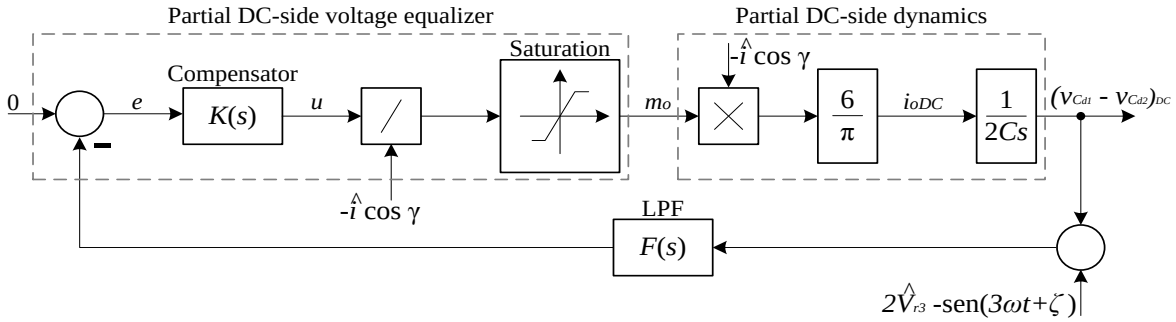


Figure 3.30. Block diagram of the neutral point voltage balancing method for SPWM modulation explained in [71].

Chapter 4: CASCADED H-BRIDGE CONVERTER

This chapter deals with the Cascaded H-Bridge (CHB) topology that is one of the most promising topologies in the medium voltage applications field. The operation of this kind of converters will be analyzed and also the most common modulation methods used to control them.

Another characteristic of this topology that will be studied in this chapter is the ability to keep working under fault conditions, which is reached thanks to the modularity of this kind of converters.

4.1. Topology description

Cascaded H-bridge topology consists on some full H-bridge cells (Figure 4.1) connected in cascade on their AC side, which compose each of the converter branches. In this way, a 3-phase CHB converter with n cells per branch looks like Figure 4.2. For correct operation of a cascaded H-bridge converter every cell needs an isolated DC source (E). These DC sources are usually equal for all cells in a branch, but there are also configurations of CHB converters with unequal DC voltages. The DC supplies are normally obtained from multi-pulse transformers (see Appendix A).

Whatever configuration of DC sources (equal or unequal) the CHB phase-to-neutral output voltage is the sum of the output (AC) voltages of all cells in a branch. For example, for the CHB converter in Figure 4.2 the voltage of branch A (v_{AN}) will be

$$v_{AN} = v_{H_{1A}} + v_{H_{2A}} + \cdots + v_{H_{nA}} \tag{4.1}$$

The voltages for branches B and C can be calculated the same way than in phase A.

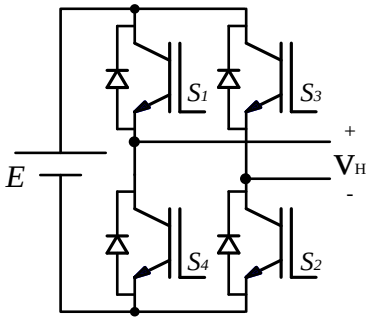


Figure 4.1. Simplified scheme of a H-bridge cell

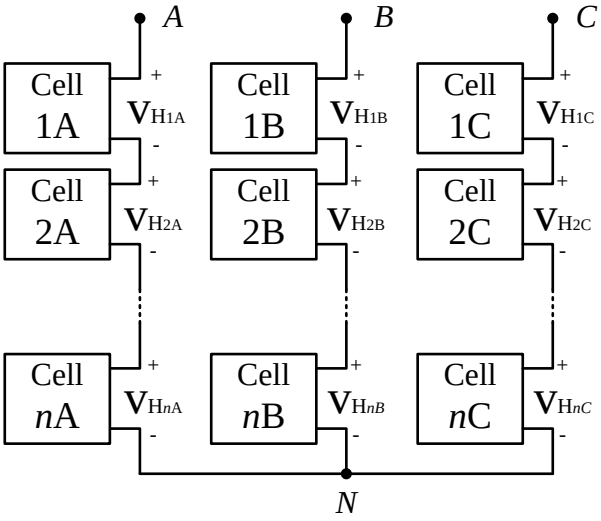


Figure 4.2. 3-phase CHB converter with 'n' cells per phase

The number of cells and the equal or unequal nature of DC sources will determine the number of levels of the phase-to-neutral voltage and ultimately the number of levels of the converter. In this way, a power converter with n H-bridge cells fed by equal DC sources will have $2n + 1$ levels.

In the case of using unequal DC sources the number of levels can be increased without increase the number of cells. In those cases it is assumed that one of the DC voltages is a multiple of the other. An example of this configuration appears in Figure 4.3. In the converter shown in Figure 4.3 the number of levels of the phase-to-neutral voltage will be $2(k + 1) + 1$, being k an integer.

Following the same philosophy, the maximum and minimum voltage levels depend on the number of cells and on the configuration of DC sources. In such way, in the case of a CHB converter with n cells fed by equal DC sources the maximum and minimum voltages will be $\pm nE$. In the case of two-cell CHB with unequal DC supplies those voltages will be $\pm (k + 1)E$.

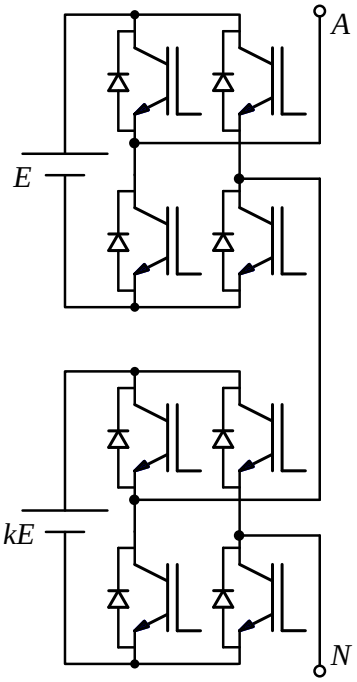


Figure 4.3. Branch A of a two-cell CHB converter with unequal DC sources

Whatever the number of cells or the configuration of DC sources in the CHB converter, the most used modulation scheme for this topology is the sinusoidal pulse-width modulation (SPWM). Next section explains the use of SPWM scheme for this kind of converter, and also other modulation methods.

4.2. Modulation methods

In this section the principal methods to modulate CHB converters are studied: the sinusoidal pulse-width modulation (SPWM), the space vector modulation (SVM) and the selective harmonic elimination (SHE).

4.2.1. Sinusoidal Pulse-Width Modulation for CHB converters

Sinusoidal Pulse-Width Modulation is the most used scheme for CHB converters. This modulation consists on comparing a sinusoidal signal with a triangular one. As already said, these waveforms are called modulation and carrier signals respectively. The carrier wave frequency is higher than the modulation signal frequency. In this way, the relationship between the carrier signal frequency and the modulation signal frequency is known as frequency modulation index, and it is calculated as

$$m_f = f_{sw}/f_m \tag{4.2}$$

where f_{sw} and f_m are the carrier signal and the modulation signal frequencies respectively.

4.2.1.1. Pulse-Width Modulation for an H-bridge

The firing signals for the converter devices are calculated through a comparison between the modulation and the carrier signals. This comparison can be done in two different ways for the H-bridge, generating each of them a kind of PWM: bipolar and unipolar.

a) Bipolar Pulse-Width Modulation

In the bipolar PWM the modulation signal is compared with one carrier signal and the result of this comparison are the firing signals for the H-bridge devices according to the following rules:

$$\begin{aligned} v_{g1} &= \begin{cases} On & if \quad v_m \geq v_c \\ Off & if \quad v_m < v_c \end{cases} \\ v_{g3} &= \overline{v_{g1}} \\ v_{g4} &= \overline{v_{g1}} \\ v_{g2} &= \overline{v_{g3}} \end{aligned} \tag{4.3}$$

where v_m is the modulation signal, v_c is the carrier signal, and v_{g1}, v_{g2}, v_{g3}, and v_{g4} are the firing signals for the devices S_1, S_2, S_3, and S_4 respectively.

This comparison is represented in Figure 4.4. As it can be seen in that figure, the output voltage signal, v_H, has two different values, E and $-E$. As all the transitions occur between these voltage levels, v_H is a bipolar signal whose harmonic content is represented in Figure 4.5. As shown in Figure 4.5, the first band of harmonics is located around the 15th harmonic, that corresponds to the value of m_f, and the multiples of this value.

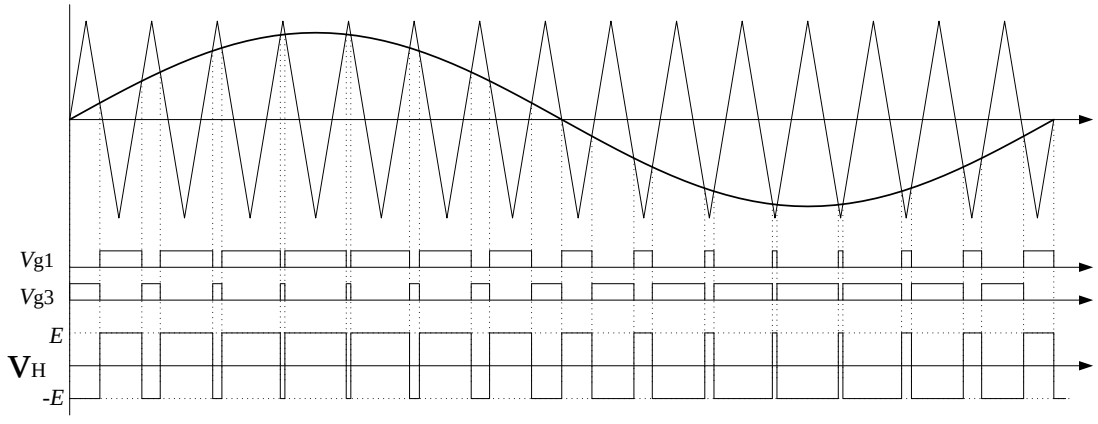


Figure 4.4. Bipolar PWM for a H-bridge cell (m_f = 15).

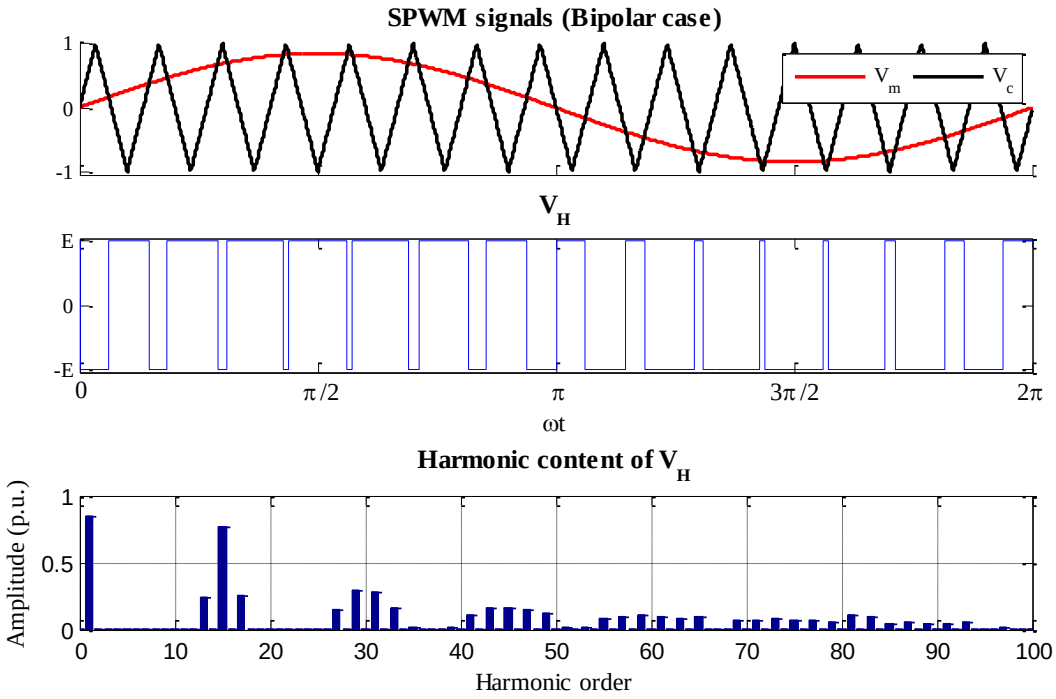


Figure 4.5. Harmonic content of the output voltage of a H-bridge using bipolar SPWM (f_m = 50 Hz, f_c = 750 Hz, m_f = 15, m_a = 0.85).

b) Unipolar Pulse-Width Modulation

There are some different ways to apply the unipolar PWM, but in this case only one of them is used and explained. In the unipolar PWM scheme used, the modulation signal is compared with one carrier signal and also with its opposite. In this case the resultant firing signals after the comparison follow these rules:

$$v_{g1} = \begin{cases} On & if \quad v_m \geq v_c \\ Off & if \quad v_m < v_c \end{cases}$$
$$v_{g3} = \begin{cases} Off & if \quad v_m \geq \overline{v_c} \\ On & if \quad v_m < \overline{v_c} \end{cases} \qquad (4.4)$$
$$v_{g4} = \overline{v_{g1}}$$
$$v_{g2} = \overline{v_{g3}}$$

where v_c is the master carrier signal and $\overline{v_c}$ is the opposite signal to v_c, or what is the same, $\overline{v_c}$ has a delay of π radians respect to v_c.

Figure 4.6 represents the unipolar comparison. In this case the output voltage signal, v_H, takes three different values, *E*, 0 and *–E*. Now there are transitions between 0 and *E*, and between 0 and *–E*, so, v_H is a unipolar signal. The harmonic content of v_H is represented in Figure 4.7, where it can be seen how now the first band of harmonics is located around the 30th harmonic, that corresponds to 2 m_f, and the multiples of this value.

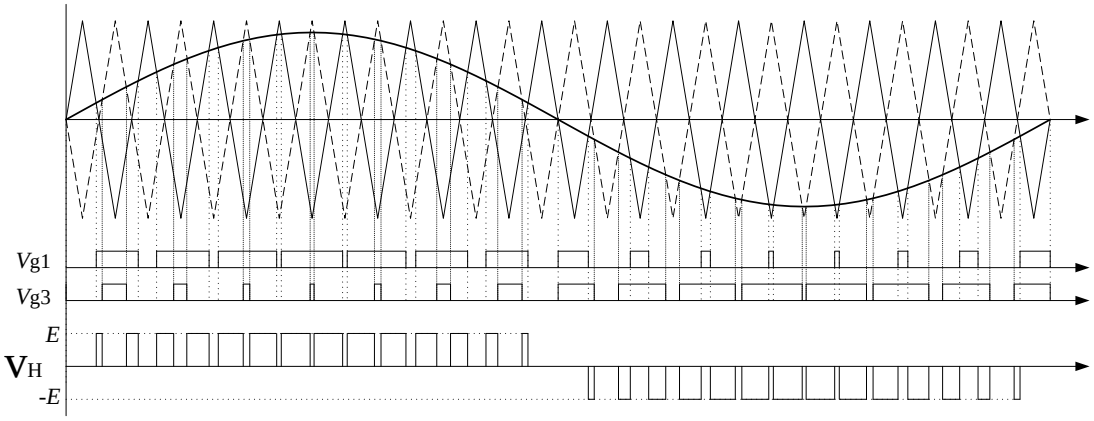


Figure 4.6. Unipolar PWM for a H-bridge cell (m_f = 15)

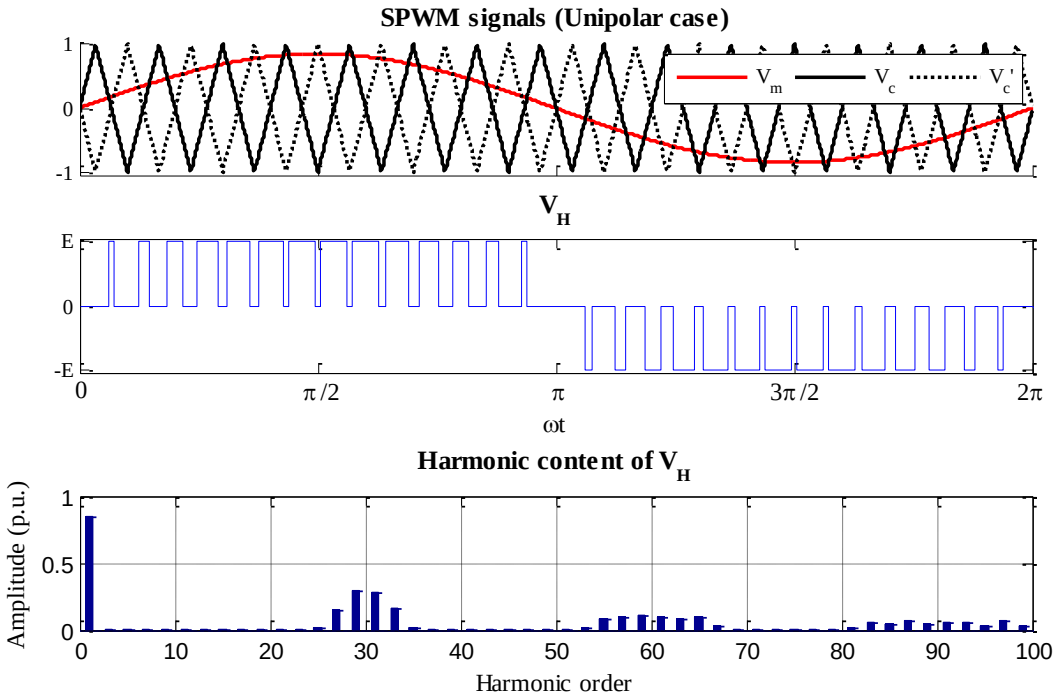


Figure 4.7. Harmonic content of the output voltage of a H-bridge using unipolar SPWM (f_m = 50 Hz, f_c = 750 Hz, m_f = 15, m_a = 0.85).

Comparing the output voltage harmonic content obtained with both cases (bipolar and unipolar), we can see some differences. The main of them is that the harmonic bands sited in the odd multiples of m_f disappear in the unipolar modulation. Figure 4.8 shows the evolution in the main harmonics' amplitude for both cases as a function of the amplitude modulation index, m_a.

The lack of harmonic band in the odd multiples of m_f in the case of unipolar modulation produces a reduction in the total harmonic distortion (THD) and in the weight total harmonic distortion (WTHD). This can be seen in Figure 4.9. As the harmonic content in the output voltage is lower using the unipolar modulation, this is the scheme that will be used in this work.

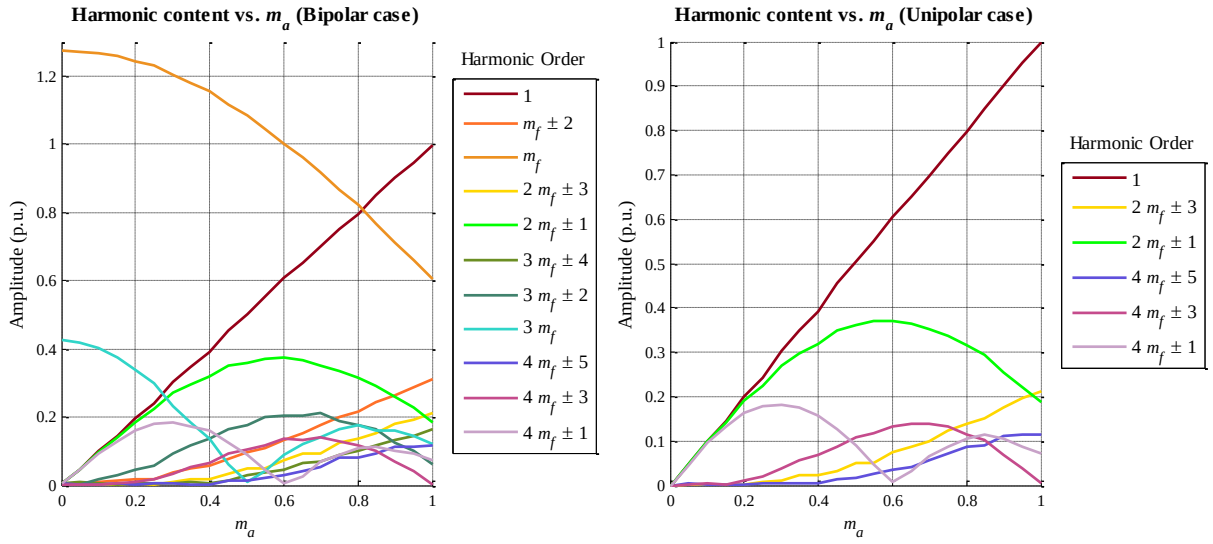


Figure 4.8. Harmonic content of the H-bridge output voltage using bipolar (left) and unipolar (right) modulation, as a function of the amplitude modulation index, m_a.

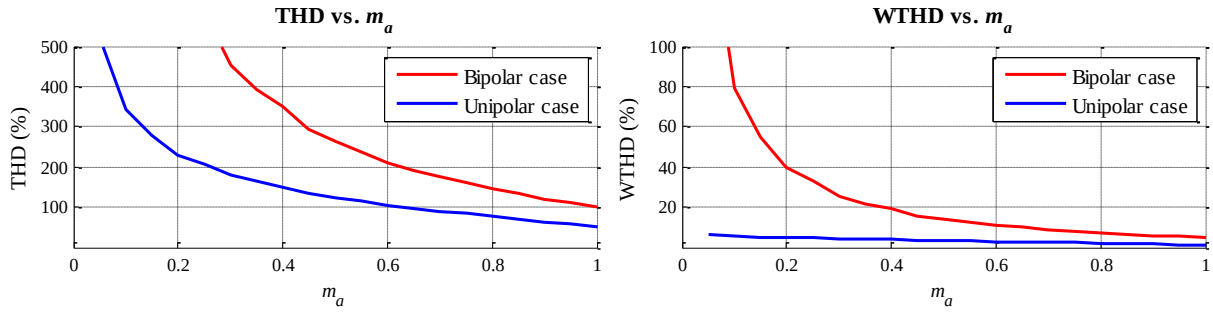


Figure 4.9. Total Harmonic Distortion (left) and Weight Total Harmonic Distortion (right) for both modulation cases (bipolar and unipolar) as a function of m_a.

4.2.1.2. Pulse-Width Modulation for a set of H-bridge cells cascaded-connected

In the case of working with a Cascaded H-bridge Converter, each one of the cells that compose it are operated following the SPWM scheme explained in subsection 4.2.1.1.b), with the peculiarity that not all the cells have the same carrier signals. From this point of view, there are two possibilities: using for the cells in a phase level-shifted carrier signals, or using phase-shift carrier signals. The last option is the most used and it has been chosen for this work, as its use allows getting a displacement of the first band of harmonics in the output signals, and also assures that all the cells in a phase operate with the same power losses independently from the modulation index.

According to that, in each phase the master carrier signal for a cell has a delay respect to the carrier signals for the other cells. This delay, δ, between the cell's carrier signals is applied in order to reduce the harmonic content in the voltage output, and it is calculated as:

$$\delta = \frac{\pi}{Num\ of\ cells\ in\ a\ phase} \tag{4.5}$$

So, the master carrier signals for each cell of a phase in the converter will be defined as follows:

$$v_{ci} = 1 - \frac{2}{\pi}\text{acos}\left[-\cos\left(m_f\omega t + \delta(i-1)\right)\right] \quad \text{for} \quad i = 1, 2, \ldots, Num\ of\ cells\ in\ a\ phase \tag{4.6}$$

and in each cell the complementary carrier signal will be

$$\overline{v_{ci}} = 1 - \frac{2}{\pi}\text{acos}\left[-\cos\left(m_f\omega t + \delta(i-1) + \pi\right)\right] \tag{4.7}$$

As an example, in a four-cells (nine-levels) CHB converter, the delay between the signals and the resultant carrier signals are the following:

$$\begin{gathered}
\delta = \pi/4 \\
v_{c1} = 1 - {}^{2}/_{\pi}\,\text{acos}\left[-\cos\left(m_f\omega t\right)\right] \\
v_{c2} = 1 - {}^{2}/_{\pi}\,\text{acos}\left[-\cos\left(m_f\omega t + \delta\right)\right] \\
v_{c3} = 1 - {}^{2}/_{\pi}\,\text{acos}\left[-\cos\left(m_f\omega t + 2\delta\right)\right] \\
v_{c4} = 1 - {}^{2}/_{\pi}\,\text{acos}\left[-\cos\left(m_f\omega t + 3\delta\right)\right] \\
\overline{v_{c1}} = 1 - {}^{2}/_{\pi}\,\text{acos}\left[-\cos\left(m_f\omega t + \pi\right)\right] \\
\overline{v_{c2}} = 1 - {}^{2}/_{\pi}\,\text{acos}\left[-\cos\left(m_f\omega t + \delta + \pi\right)\right] \\
\overline{v_{c3}} = 1 - {}^{2}/_{\pi}\,\text{acos}\left[-\cos\left(m_f\omega t + 2\delta + \pi\right)\right] \\
\overline{v_{c4}} = 1 - {}^{2}/_{\pi}\,\text{acos}\left[-\cos\left(m_f\omega t + 3\delta + \pi\right)\right]
\end{gathered} \tag{4.8}$$

The previous example is illustrated in Figure 4.10.

For clarity, only the master carrier of each cell has been represented. The complementary carrier in each case is obtained applying a delay of π radians.

In Figure 4.10 it can be observed that the output phase-to-neutral voltage has its first band of harmonics around the 120th harmonic, that is 8 m_f, as it is a four-cells converter. In general, the first band of harmonics of the phase-to-neutral voltage in a CHB converter will be located around 2 · '*Num of cells per phase*' · m_f.

If the first and second harmonic bands (around 120th and 240th harmonics) are analyzed (Figure 4.11), it can be seen that the number of harmonics that compose those bands is greater

than in the case of a single cell (see Figure 4.8-rigth), but these harmonics are further from the fundamental one, and their amplitudes are also lower. So, the cascade connection of H-bridges supposes an improvement in this aspect.

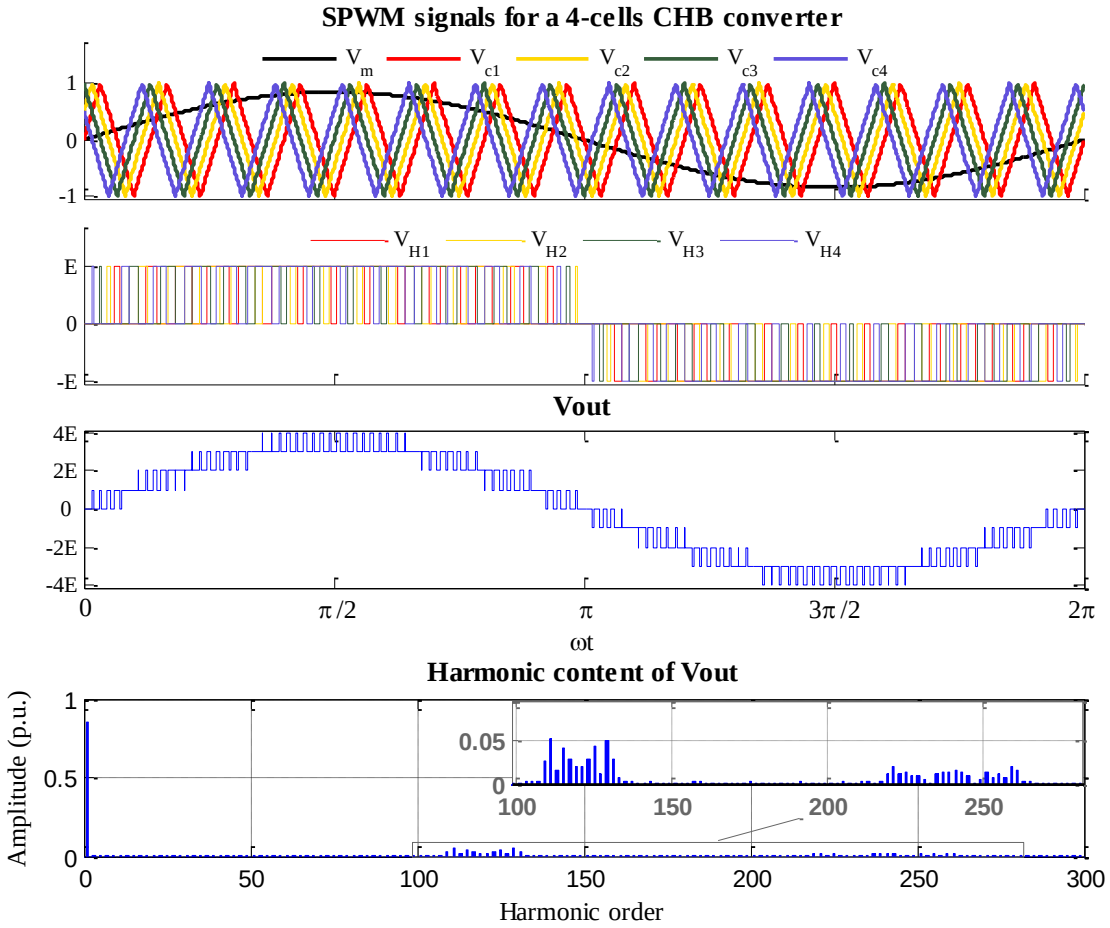


Figure 4.10. Example of PWM for a nine-level (four-cells) CHB converter (mf = 15, ma = 0.85). (Note that for clarity purposes only the master carrier signals have been depicted).

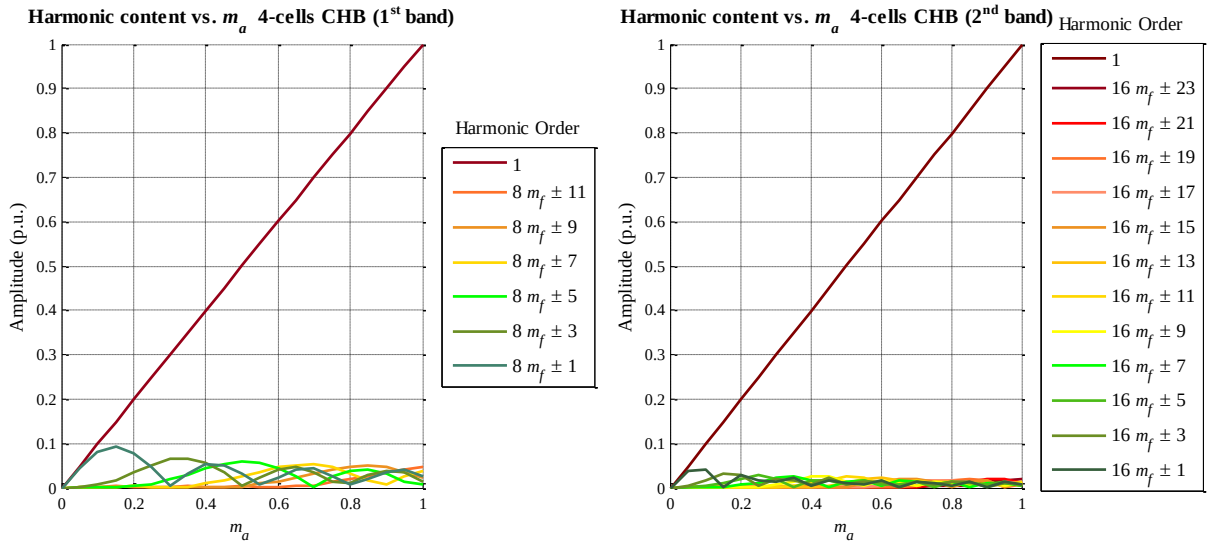


Figure 4.11. Amplitude analysis of harmonics in the first band (left) and the second band (right) versus m_a in a four-cells CHB converter.

4.2.2. Space Vector Modulation

The Space Vector Modulation for multilevel converters is based on the same principia that for two or three-level inverters: the representation of the voltage reference vector as a combination of fixed space vectors that represent the converter switching states. But in the case of multilevel converters the total number of vectors in the space is higher, as it depends on the number of levels in the converter. In this way, for a *n*-level converter, the number of switching states is n^3, the number of space vectors is $1 + \sum_{i=0}^{n-1} 6 \cdot i$, and those vectors divides the space hexagon in $6(n\text{-}1)^2$ triangles. The complexity growing process as the number of levels increases is illustrated in Figure 4.12.

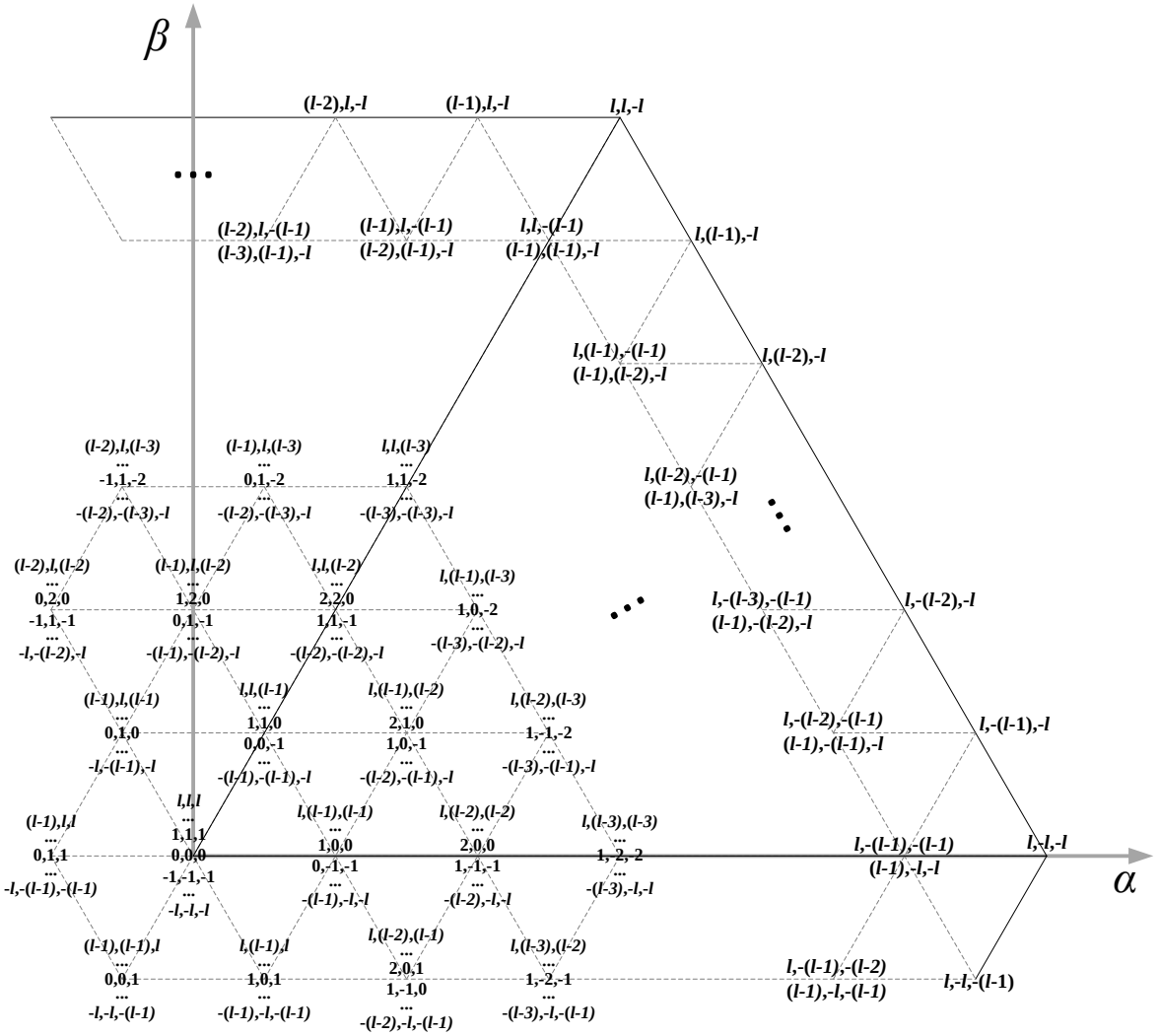


Figure 4.12. Detail of the Space Vector hexagon for a generic n-level converter (where l represents the maximum voltage level of the converter: l = (n-1)/2.

Figure 4.12 illustrates that there are several possible combinations of switching states which generate the same output voltage. However, as the amplitude of the reference voltage increases, the possible combinations of switching states are reduced. One of the advantages of having some switching combinations for the same voltage vector is that this fact allows

operating the converter under fault conditions, as it will be explained in a following subsection.

Space vector modulation provides more flexibility to optimize switching waveforms due to the existence of redundant switching states and adjustable duty cycles, and it is a method suitable to be digitally implemented [72]. However, the main drawback of applying SVM to multilevel converters is that the complexity of the algorithm highly grows with the number of levels as it has been mentioned earlier.

With the aim to reduce this complexity, several methods have been proposed in the technical literature. Most of the proposed methods are based on coordinate transformations which simplify the calculation of the space vectors [73]-[76]. However, there is another approach which avoids the coordinate transformations and performs the vector calculation in the conventional orthogonal coordinate system [77]-[80]. As space vector modulation follows the same principia for all the multilevel converters, this approach will be described in depth in the chapter related to the modular multilevel converter (subsection 5.2.2).

4.2.3. Selective Harmonic Elimination for CHB converters

As was explained in subsection 3.2.3, selective harmonic elimination consists on calculating off-line the angles in which switching events occur, and then using those angles to produce the switching events in the converter in order to eliminate a chosen number of harmonics following the fundamental one.

For multilevel converters, as the cascaded H-bridge, the angles calculating process is similar to the explained previously, but with the particularity that in this case, as the signals have more levels, the equations are different. The general expression for the harmonic amplitude, h_n, of a multilevel waveform is the following:

$$h_n = \frac{4E}{n\pi}\Big[\cos(n\theta_1) - \cos(n\theta_2) + \cdots + \cos\left(n\theta_{k_1}\right) + \cos\left(n\theta_{k_1+1}\right) - \cos\left(n\theta_{k_1+2}\right) + \cdots + \cos\left(n\theta_{k_{(L-1)}+1}\right) - \cos\left(n\theta_{k_{(L-1)}+2}\right) + \ldots + (-1)^{N+1}\cdot\cos(n\theta_N)\Big] \tag{4.9}$$

Where n is the harmonic order, E is the voltage step between the different levels in the output signal, θ_1, θ_2, …, θ_{k1}, are the switching angles between zero-level and the first level, θ_{k1+1}, θ_{k1+2}, …, θ_{k2}, are the switching angles between the first and second levels, $\theta_{k(L-1)+1}$, $\theta_{k(L-1)+2}$, …, θ_N, are the switching angles between the two top levels. In this way, L is the maximum level, and the total number of levels in the converter (n) is equal to $2L+1$. In the same way, k_1, k_2, …, $k_{(L-1)}$ are the number of switching angles between two consecutive voltage levels, and the number of switching events in a quarter of period, N, is the sum of these values, and it determines the number of harmonics that will be eliminated.

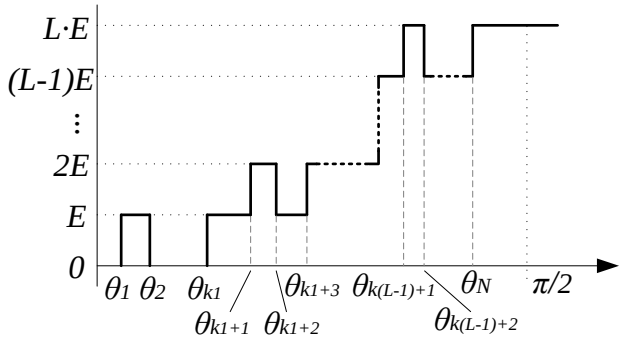


Figure 4.13. Generic multilevel waveform.

As it can be seen in Figure 4.13, k_1, k_2, …, $k_{(L-1)}$, must be always even, meanwhile k_L can be odd or even. So, N can also be an odd or even number.

According to equation (4.9), for a set of N angles the equation system to be solved for a multilevel converter will be the following:

$$\begin{aligned}
f_1(\theta) &= \cos(\theta_1) - \cos(\theta_2) + \cdots + \cos\left(\theta_{k_1}\right) + \cos\left(\theta_{k_1+1}\right) - \cos\left(\theta_{k_1+2}\right) + \cdots \\
&\quad + \cos\left(\theta_{k_{(L-1)}+1}\right) - \cos\left(\theta_{k_{(L-1)}+2}\right) + \cdots + (-1)^{N+1} \cdot \cos(\theta_N) = \frac{\pi E}{4} m \\
f_2(\theta) &= \cos(5\theta_1) - \cos(5\theta_2) + \cdots + \cos\left(5\theta_{k_1}\right) + \cos\left(5\theta_{k_1+1}\right) - \cos\left(5\theta_{k_1+2}\right) + \cdots \\
&\quad + \cos\left(5\theta_{k_{(L-1)}+1}\right) - \cos\left(5\theta_{k_{(L-1)}+2}\right) + \cdots + (-1)^{N+1} \cdot \cos(5\theta_N) = 0 \\
f_3(\theta) &= \cos(7\theta_1) - \cos(7\theta_2) + \cdots + \cos\left(7\theta_{k_1}\right) + \cos\left(7\theta_{k_1+1}\right) - \cos\left(7\theta_{k_1+2}\right) + \cdots \\
&\quad + \cos\left(7\theta_{k_{(L-1)}+1}\right) - \cos\left(7\theta_{k_{(L-1)}+2}\right) + \cdots + (-1)^{N+1} \cdot \cos(7\theta_N) = 0 \\
&\vdots \\
f_N(\theta) &= \cos(X\theta_1) - \cos(X\theta_2) + \cdots + \cos\left(X\theta_{k_1}\right) + \cos\left(X\theta_{k_1+1}\right) - \cos\left(X\theta_{k_1+2}\right) + \cdots \\
&\quad + \cos\left(X\theta_{k_{(L-1)}+1}\right) - \cos\left(X\theta_{k_{(L-1)}+2}\right) + \cdots + (-1)^{N+1} \cdot \cos(X\theta_N) = 0
\end{aligned} \tag{4.10}$$

$$X = \begin{cases} 3N-1 & for\ N\ even \\ 3N-2 & for\ N\ odd \end{cases}$$

As in the case of two or three-level inverters, the main problem of SHE lies in solving the non-linear transcendental equations. Once again, for this task some approximation methods can be used, and also other methods like resultant theory.

4.2.3.1. Stair-case SHE for CHB converters

A particular case of harmonic elimination for multilevel converters is the stair-case SHE modulation. In this particular case the number of calculated switching angles in a quarter of period for an *n*-level converter is (*n*-1)/2, what means that for a CHB converter the number of angles in a quarter of period is the same as the number of cells in the converter. Figure 4.14

illustrates the principle of working in this type of modulation, in which each IGBT in each cell works at the fundamental frequency.

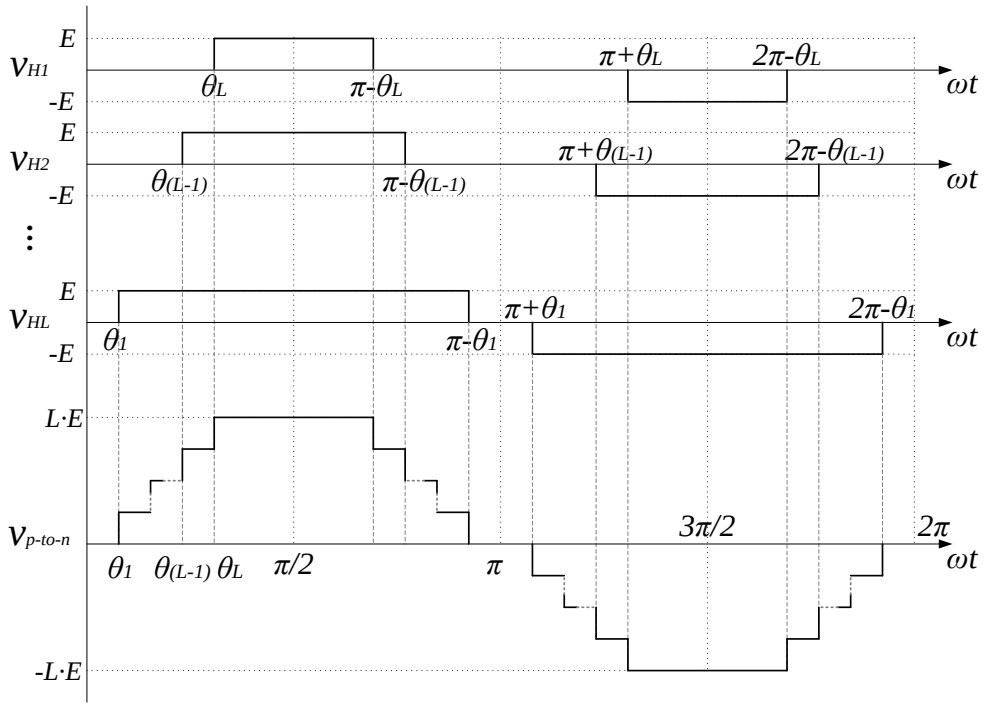


Figure 4.14. Stair-case general waveform for a CHB converter with L = (n-1)/2 cells (n-level).

For example, for a CHB that has four cells per phase four angles would be calculated and harmonics 5th, 7th, and 11th would be eliminated. In these conditions, the switching angles for a four-cells nine-level converter are calculated by solving the following equations system:

$$\begin{cases} \cos\theta_1 + \cos\theta_2 + \cos\theta_3 + \cos\theta_4 = \dfrac{\pi E}{4} m \\ \cos 5\theta_1 + \cos 5\theta_2 + \cos 5\theta_3 + \cos 5\theta_4 = 0 \\ \cos 7\theta_1 + \cos 7\theta_2 + \cos 7\theta_3 + \cos 7\theta_4 = 0 \\ \cos 11\theta_1 + \cos 11\theta_2 + \cos 11\theta_3 + \cos 11\theta_4 = 0 \end{cases} \tag{4.11}$$

with the usual constraint: $0 < \theta_1 < \theta_2 < \theta_3 < \theta_4 < {}^{\pi}/_{2}$.

Equations in (4.11) can be transformed into polynomials through a change of variables:

$$x_1 = \cos\theta_1 ; \;\; x_2 = \cos\theta_2 ; \;\; x_3 = \cos\theta_3 ; \;\; x_4 = \cos\theta_4 \tag{4.12}$$

On the other hand, the cosine of the multiple of an angle can be calculated using the following trigonometrical identities

$$\begin{aligned} \cos 5\alpha &= 16\cos^5\alpha - 20\cos^3\alpha + 5\cos\alpha \\ \cos 7\alpha &= 64\cos^7\alpha - 112\cos^5\alpha + 56\cos^3\alpha - 7\cos\alpha \end{aligned} \tag{4.13}$$

$$\cos 11\alpha = 1024\cos^{11}\alpha - 2816\cos^{9}\alpha + 2816\cos^{7}\alpha - 1232\cos^{5}\alpha + 220\cos^{3}\alpha - 11\cos\alpha$$

Applying in (4.11) the changes described in (4.12) and (4.13), the non-linear and transcendental equations system becomes a polynomial system:

$$\begin{aligned}
f_1(x) &= x_1 + x_2 + x_3 + x_4 = \frac{\pi E}{4} m \\
f_2(x) &= 16\,{x_1}^5 - 20\,{x_1}^3 + 5\,x_1 + 16\,{x_2}^5 - 20\,{x_2}^3 + 5\,x_2 + 16\,{x_3}^5 - 20\,{x_3}^3 + 5\,x_3 \\
&\quad + 16\,{x_4}^5 - 20\,{x_4}^3 + 5\,x_4 = 0 \\
f_3(x) &= 64\,{x_1}^7 - 112\,{x_1}^5 + 56\,{x_1}^3 - 7\,x_1 + 64\,{x_2}^7 - 112\,{x_2}^5 + 56\,{x_2}^3 - 7\,x_3 + 64\,{x_3}^7 \\
&\quad - 112\,{x_3}^5 + 56\,{x_3}^3 - 7\,x_3 + 64\,{x_4}^7 - 112\,{x_4}^5 + 56\,{x_4}^3 - 7\,x_4 = 0 \\
f_4(x) &= 1024\,{x_1}^{11} - 2816\,{x_1}^9 + 2816\,{x_1}^7 - 1232\,{x_1}^5 + 220\,{x_1}^3 - 11\,x_1 + 1024\,{x_2}^{11} \\
&\quad - 2816\,{x_2}^9 + 2816\,{x_2}^7 - 1232\,{x_2}^5 + 220\,{x_2}^3 - 11\,x_2 + 1024\,{x_3}^{11} \\
&\quad - 2816\,{x_3}^9 + 2816\,{x_3}^7 - 1232\,{x_3}^5 + 220\,{x_3}^3 - 11\,x_3 + 1024\,{x_4}^{11} \\
&\quad - 2816\,{x_4}^9 + 2816\,{x_4}^7 - 1232\,{x_4}^5 + 220\,{x_4}^3 - 11\,x_4 = 0
\end{aligned} \tag{4.14}$$

Figure 4.15 shows a solution of the equation system in (4.14), that is a solution for the 4-cells (9-levels) CHB stair-case problem.

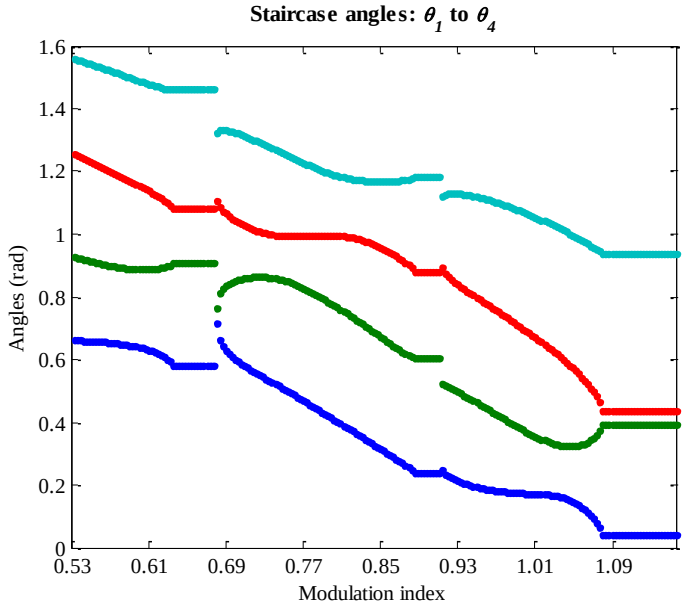


Figure 4.15. Stair-case solution for a 4-cells CHB converter.

In addition, in Figure 4.16 the output phase-to-neutral and phase-to-phase voltages are shown. As it can be seen, in the phase-to-neutral voltage exist 3rd and 9th harmonics, but in the phase-to-phase voltage these harmonics disappear at the same time that 5th, 7th, and 11th harmonics are eliminated, and the first harmonic to appear is 13th.

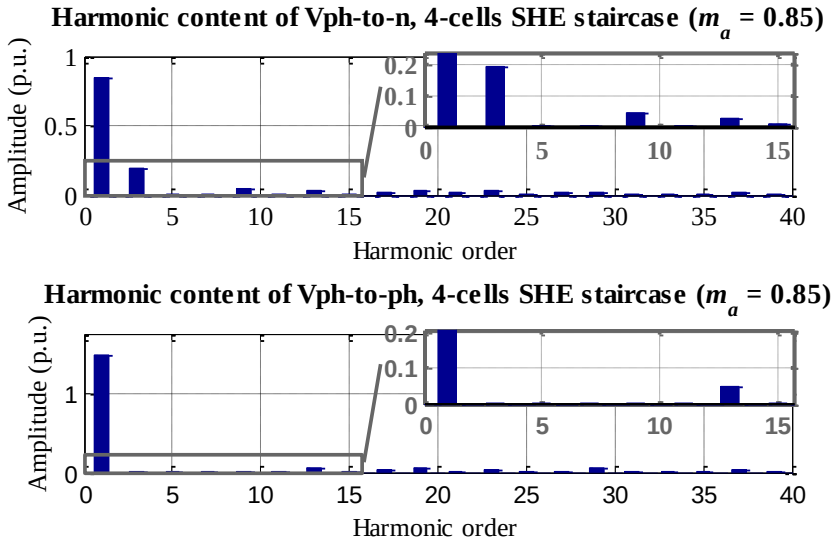


Figure 4.16. Harmonic content of the phase-to-neutral (up) and the phase-to-phase (down) voltages when Staircase-SHE modulation is applied to a 4-cells CHB converter (m_a = 0.85).

4.3. CHB operation with faulty cells

There are some kinds of faults that can occur in a CHB converter. In this Thesis the author focuses in those faults that may disable a cell and in the methods that allows keeping the converter operation.

A fault in one (or more) of the devices that composed the converter will be detected if the communication with its corresponding driver is lost. If there is a faulty device two situations are possible: that it remains as an open-circuit or as short-circuit. If the device remains in open-circuit the only requirement is to close the output cell bypass in order to guarantee a path for the current. But if the device remains as short-circuit there is a risk to damage the multi-pulse transformer as the rectifier output will be in short-circuit. To avoid this risk it is advisable to connect fuses in the rectifiers input in order to limit the current that demands the rectifier. In this Thesis including a braking chopper in each cell has not been considered. So, if in a drive in application a fault occurs in a braking situation, it could produce a situation of overvoltage in the DC capacitors of all the cells. For this reason the lack of braking choppers in the cells must be compensated oversizing the capacitors.

According to the previous, in case of happen a fault in a cell, if it is desired to keep the operation, the first step is to bypass this cell in its AC side in order to keep a path for the output current. The bypassing of a cell means that the corresponding phase is able to supply voltage with less amplitude than the other two. Moreover the supplied phase-to-phase voltages in this case will not be balanced. That is the reason why it is advisable to implement one of the voltage balancing methods that will be explained in the following subsections.

4.3.1. Bypassing cells of the same level

The first solution that one can think to balance the line-to-line voltages when a cell fails in a branch is to bypass also the corresponding cells in the other branches. For example, in Figure 4.17 is illustrated the case of a six-cells per branch (thirteen-level) CHB converter with two faulty cells in the same branch: '5C' and '6C'.

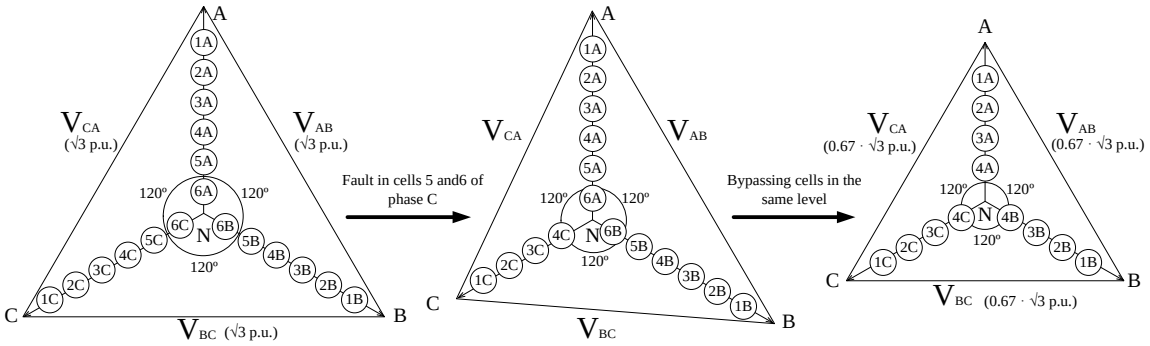


Figure 4.17. Illustration of bypassing the cells of the same level in a six-cells CHB converter.

Table 4.1. Available output voltage for the CHB converter depending on the number of bypassed cells, for converters with 2, 3, 4, 5, 6, 7 and 8 cells per phase, when the cells in the same level are bypassed too.

Available cells in phase A	Available cells in phase B	Available cells in phase C	Available output voltage (% V_{max})	Available cells in phase A	Available cells in phase B	Available cells in phase C	Available output voltage (% V_{max})
Number of cells per phase = 2				***Number of cells per phase = 3***			
2	2	2	100	3	3	3	100
2	2	1	50	3	3	2	66.67
2	2	0	0	3	3	1	33.33
Number of cells per phase = 4				3	3	0	0
4	4	4	100	***Number of cells per phase = 7***			
4	4	3	75	7	7	7	100
4	4	2	50	7	7	6	85.71
4	4	1	25	7	7	5	71.43
4	4	0	0	7	7	4	57.14
Number of cells per phase = 5				7	7	3	42.86
5	5	5	100	7	7	2	28.57
5	5	4	80	7	7	1	14.29
5	5	3	60	7	7	0	0
5	5	2	40	***Number of cells per phase = 8***			
5	5	1	20	8	8	8	100
5	5	0	0	8	8	7	87.5
Number of cells per phase = 6				8	8	6	75
6	6	6	100	8	8	5	62.5
6	6	5	83.33	8	8	4	50
6	6	4	66.67	8	8	3	37.5
6	6	3	50	8	8	2	25
6	6	2	33.33	8	8	1	12.5
6	6	1	16.67	8	8	0	0
6	6	0	0				

Doing those bypasses the balance between the line-to-line voltages is achieved, but the problem is that the available output voltage is reduced, especially when there are some faulty cells in a branch. This effect is shown in Table 4.1, where appear the maximum available voltages depending on the number of bypassed cells in each phase of the converter. (The table is done considering that phase A is where there are less bypassed cells, phase B is the second branch where there are less bypassed cells, and the higher number of bypassed cells are in phase C.)

From Table 4.1 it can be concluded that bypassing the corresponding cells in the other phases is not the better choice to balance the phase-to-phase output voltage because in most cases the available voltage is reduced significantly when only one cell is bypassed.

4.3.2. Space Vector Modulation with redundant switching states

Another method to balance the output voltages is to use the space vector modulation taking advantage of the redundant switching states. Examples using this technique can be found in [81]-[34].

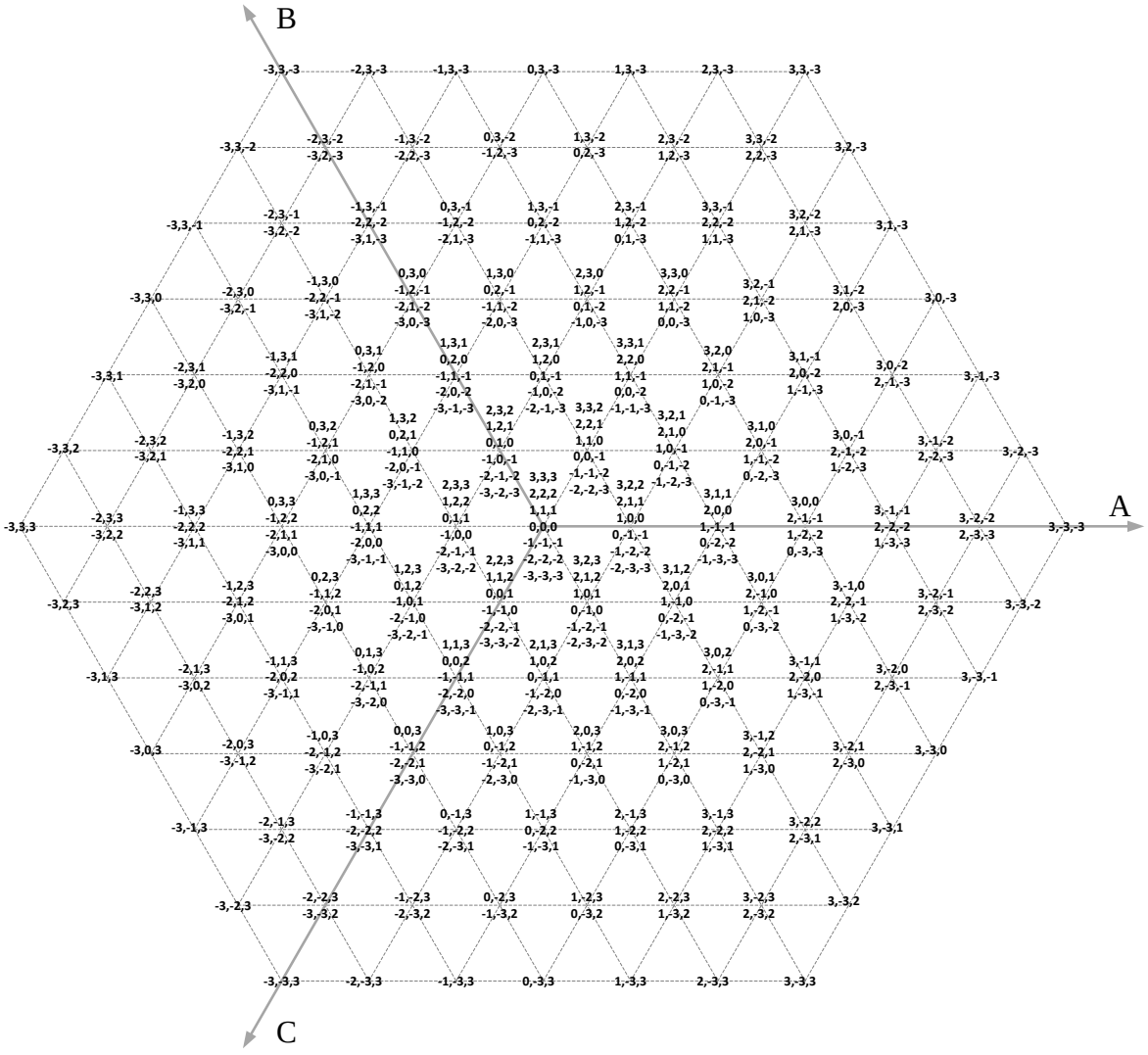


Figure 4.18. Space vectors hexagon for a seven-level CHB converter.

The space vectors hexagon for a cascaded H-bridge converter is as complex as the number of levels the converter has. For example, Figure 4.18 shows the hexagon corresponding to a seven-level cascaded H-bridge. In that figure the switching states for each vector are indicated.

When there is a faulty cell the space vector hexagon is modified, the number of valid switching states decrease, this effect can be seen in Figure 4.19, where the shaded zone in each case indicates the available vectors. Those vectors have at least one valid switching state. In each case the red hexagon indicates the zone in which all the space vectors have, at least, one valid state that guaranties a balanced phase-to-phase voltage.

Extending what has been explained above for a three-cells CHB to converters with a different number of cells, Table 4.2 indicates the available phase-to-phase output voltage with this balancing method.

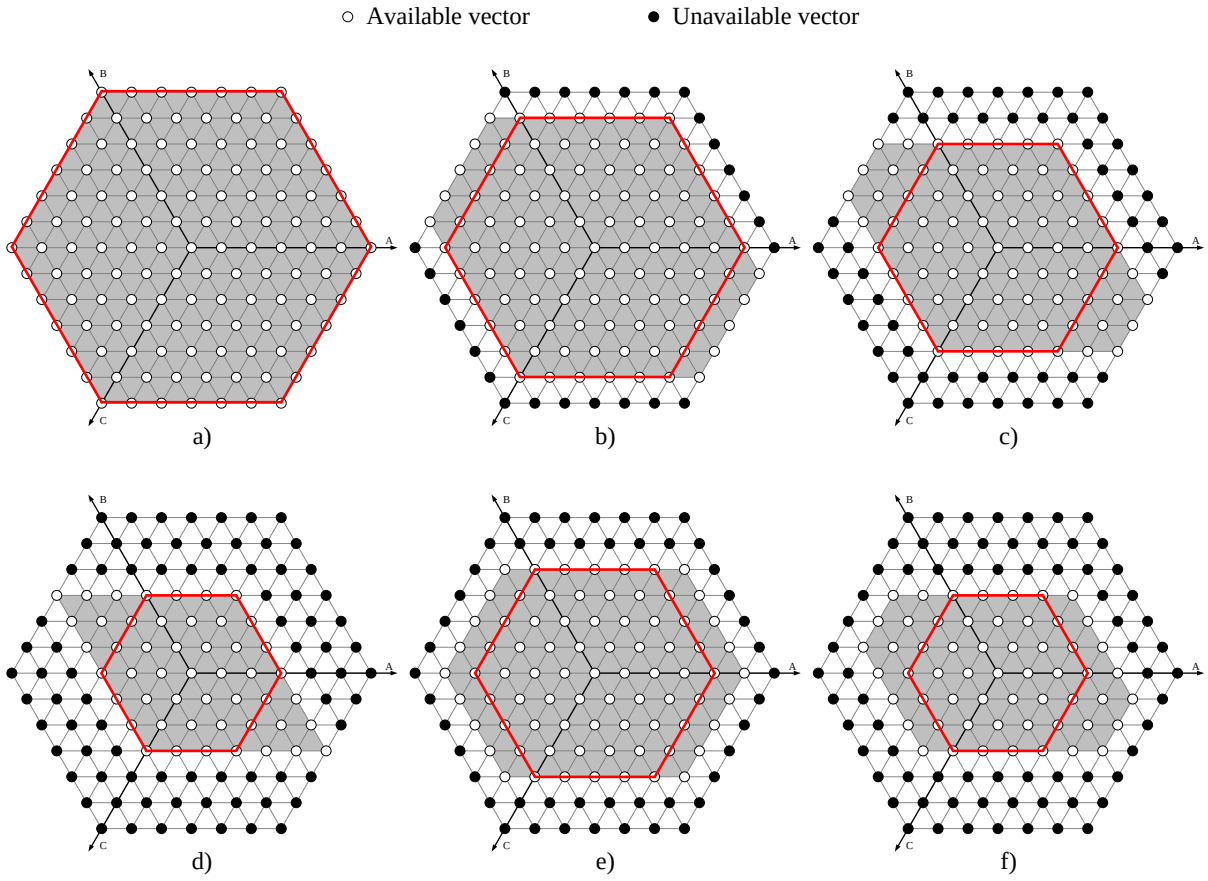


Figure 4.19. Representation of the valid switching states for a 7-levels CHB converter in normal operation (a), with one faulty cell in phase C (b), with two faulty cells in phase C (c), with three faulty cells in phase C (d), with one faulty cell in phase C and another one in phase B (e), and with two faulty cells in phase C and one in phase B (f).

Although using space vector modulation in this kind of converters has a high complexity, it can be seen from Table 4.2 that with this strategy the use of the remaining cells is better improved than in the previous case (Table 4.1).

Table 4.2. Available phase-to-phase output voltage for the CHB converter depending on the number of faulty cells, for converters with 2, 3, 4, 5, 6, 7 and 8 cells per phase, when redundant switching states are used.

Available cells in phase A	Available cells in phase B	Available cells in phase C	Available output voltage (% V_{max})
Number of cells per phase = 2			
2	2	2	100
2	2	1	75
2	2	0	50
2	1	1	50
2	1	0	25
2	0	0	0
Number of cells per phase = 3			
3	3	3	100
3	3	2	83.33
3	3	1	66.67
3	3	0	50
3	2	2	66.67
3	2	1	50
3	2	0	33.33
3	1	1	33.33
3	1	0	16.67
3	0	0	0
Number of cells per phase = 4			
4	4	4	100
4	4	3	87.5
4	4	2	75
4	4	1	62.5
4	4	0	50
4	3	3	75
4	3	2	62.5
4	3	1	50
4	3	0	37.5
4	2	2	50
4	2	1	37.5
4	2	0	25
4	1	1	25
4	1	0	12.5
4	0	0	0
Number of cells per phase = 5			
5	5	5	100
5	5	4	90
5	5	3	80
5	5	2	70
5	5	1	60
5	5	0	50
5	4	4	80
5	4	3	70
5	4	2	60
5	4	1	50
5	4	0	40
Number of cells per phase = 7			
7	7	7	100
7	7	6	92.86
7	7	5	85.71
7	7	4	78.57
7	7	3	71.43
7	7	2	64.29
7	7	1	57.14
7	7	0	50
7	6	6	85.71
7	6	5	78.57
7	6	4	71.43
7	6	3	64.29
7	6	2	57.14
7	6	1	50
7	6	0	42.86
7	5	5	71.43
7	5	4	64.29
7	5	3	57.14
7	5	2	50
7	5	1	42.86
7	5	0	35.71
7	4	4	57.14
7	4	3	50
7	4	2	42.86
7	4	1	35.71
7	4	0	28.57
7	3	3	42.86
7	3	2	35.71
7	3	1	28.57
7	3	0	21.43
7	2	2	28.57
7	2	1	21.43
7	2	0	14.29
7	1	1	14.29
7	1	0	7.14
7	0	0	0
Number of cells per phase = 8			
8	8	8	100
8	8	7	93.75
8	8	6	87.5
8	8	5	81.25
8	8	4	75
8	8	3	68.75
8	8	2	62.5
8	8	1	56.25

Available cells in phase A	Available cells in phase B	Available cells in phase C	Available output voltage (% V_{max})	Available cells in phase A	Available cells in phase B	Available cells in phase C	Available output voltage (% V_{max})
5	3	3	60	8	8	0	50
5	3	2	50	8	7	7	87.5
5	3	1	40	8	7	6	81.25
5	3	0	30	8	7	5	75
5	2	2	40	8	7	4	68.75
5	2	1	30	8	7	3	62.5
5	2	0	20	8	7	2	56.25
5	1	1	20	8	7	1	50
5	1	0	10	8	7	0	43.75
5	0	0	0	8	6	6	75
Number of cells per phase = 6				8	6	5	68.75
6	6	6	100	8	6	4	62.5
6	6	5	91.67	8	6	3	56.25
6	6	4	83.33	8	6	2	50
6	6	3	75	8	6	1	43.75
6	6	2	66.67	8	6	0	37.5
6	6	1	58.33	8	5	5	62.5
6	6	0	50	8	5	4	56.25
6	5	5	83.33	8	5	3	50
6	5	4	75	8	5	2	43.75
6	5	3	66.67	8	5	1	37.5
6	5	2	58.33	8	5	0	31.25
6	5	1	50	8	4	4	50
6	5	0	41.67	8	4	3	43.75
6	4	4	66.67	8	4	2	37.5
6	4	3	58.33	8	4	1	31.25
6	4	2	50	8	4	0	25
6	4	1	41.67	8	3	3	37.5
6	4	0	33.33	8	3	2	31.25
6	3	3	50	8	3	1	25
6	3	2	41.67	8	3	0	18.75
6	3	1	33.33	8	2	2	25
6	3	0	25	8	2	1	18.75
6	2	2	33.33	8	2	0	12.5
6	2	1	25	8	1	1	12.5
6	2	0	16.67	8	1	0	6.25
6	1	1	16.67	8	0	0	0
6	1	0	8.33				
6	0	0	0				

4.3.3. Using variable DC voltages

As said previously, the DC voltages of all the cells in a CHB converter must be isolated from each other. In the case of using independent adjustable DC sources, if a fault occurs in one cell (or more), the DC voltages of the remaining cells in the same phase can be increased in order to allow these cells supply the AC voltage that the faulty-cell cannot supply.

If the individual DC voltages are obtained from a multi-winding transformer, there is the possibility of using controlled rectifiers to supply variable DC voltages and achieve balanced phase-to-phase voltages in case of faulty-cell, as in [84].

For CHB converters used in grid-connected applications, another option for balancing phase-to-phase output voltages when there are faulty-cells is to control the DC voltage level through the cells AC side, as it is done in [85].

4.3.4. Neutral shift method

The neutral shift method consists on bypassing the faulty cells and adjusting the amplitudes and phases of the remaining branches phase-to-neutral voltages in order to balance the line-to-line output voltages, such as is represented in Figure 4.20. Comparing Figure 4.17 and Figure 4.20 it can be seen how with this balancing method the 'sane'-cells are better exploited, as the 88% of the maximum voltage can be supplied with two faulty-cells, instead of the 66,67% that was supplied in the same conditions with the bypassing method.

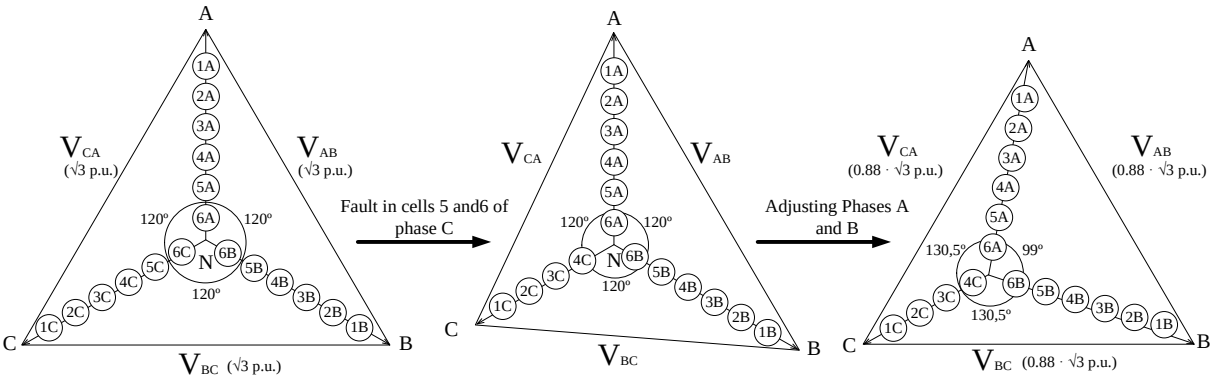


Figure 4.20. Illustration of neutral shift method in a six-cells CHB converter.

There are many examples of using this method to balance the output voltages in a CHB converter: In [37] a control loop is presented to achieve the neutral shift. In [84] the neutral shift method is combined with the possibility of controllable DC voltages in order to have a better balanced response than only with the neutral shift method. In [86] the neutral shift is achieved through pre-calculated angles tables.

What is done in the neutral-shift method proposed in this work is calculating directly the phase-to-neutral voltage of each branch considering the desired output balanced phase-to-phase voltage and the number of available cells in each branch. The method follows these steps:

a) Check if the reference output voltage can be achieved with the available cells, for which the following restriction must be satisfied: $V_{ref} \leq V_{max}$.

b) If the previous step is satisfied, the amplitude and phase of the phase-to-neutral voltages are calculated. If not, the maximum available phase-to-neutral voltages that result in balanced phase-to-phase voltages are fixed. The phase-to-neutral voltages are calculated mathematically assuring that the triangle in Figure 4.21 is equilateral, which is the same as saying that the phase-to-phase output voltages are balanced.

c) Once the phase-to-neutral voltage vectors $\boldsymbol{V_A}$, $\boldsymbol{V_B}$, and $\boldsymbol{V_C}$ (amplitude and phase) are known appropriate modulation signals are calculated for each branch.

d) The sinusoidal PWM scheme is applied using the modulation signals generated previously.

All this process is illustrated in the block diagram shown in Figure 4.22.

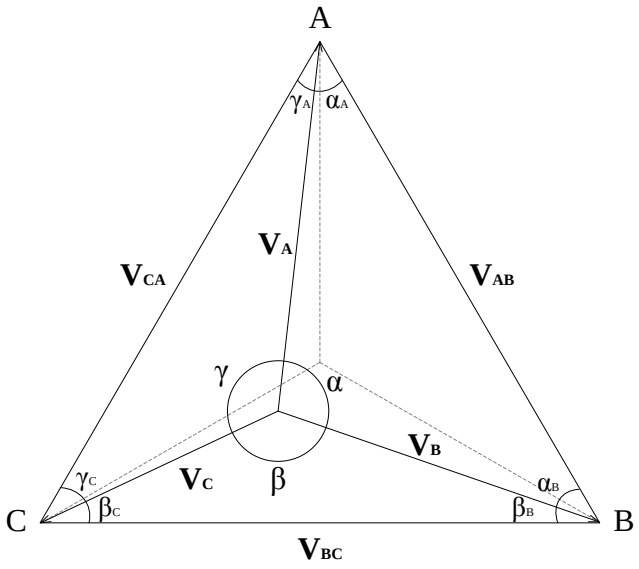


Figure 4.21. Representation of the phase-to-neutral voltages calculation.

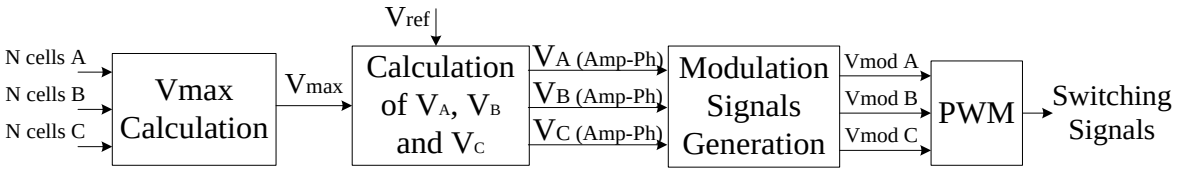


Figure 4.22. Block diagram of the proposed neutral-shift method.

In step a) V_{max} is the maximum balanced phase-to-phase available voltage, and it is calculated as follows:

$$V_{max} = \sqrt{\frac{{a_{max}}^2 + {b_{max}}^2 + {c_{max}}^2 + \sqrt{3\,r}}{2}} \tag{4.15}$$

$$r = -{a_{max}}^4 - {b_{max}}^4 - {c_{max}}^4 + 2{a_{max}}^2{b_{max}}^2 + 2{a_{max}}^2{c_{max}}^2 + 2{b_{max}}^2{c_{max}}^2$$

where $a_{max}, b_{max}, c_{max}$ represent the maximum per unit (p. u.) voltage that each branch can deliver, N_A, N_B, N_C are the number of available cells in each branch and $N_{cellsBranch}$ the original total number of cells in a branch.

With the aim to reduce the computational complexity of this method, the equation (4.15) can be transformed in a simpler expression using the Heron's formula. Heron's formula defines the area of a triangle (*A*) which sides are *x*, *y*, and *z*, as:

$$A = \frac{1}{4}\sqrt{(x+y+z)(-x+y+z)(x-y+z)(x+y-z)} \tag{4.16}$$

Equation (4.16) can be re-written as:

$$A = \frac{1}{4}\sqrt{-x^4 - y^4 - z^4 + 2x^2y^2 + 2x^2z^2 + 2y^2z^2} \tag{4.17}$$

Considering (4.17), we can see that the radicand is a similar expression to which was named *r* in (4.15). So $\sqrt{r}$ is equal to four times the area of a triangle which sides are a_{max}, b_{max} and c_{max}.

On the other hand, the area of a triangle composed of sides *x*, *y*, and *z* (see Figure 4.23) also can be calculated as half of the product between its base and its height:

$$A = \frac{1}{2}\,yh \tag{4.18}$$

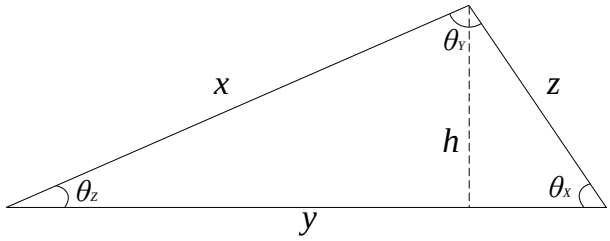


Figure 4.23. Illustration of a generic triangle of sides x, y, z.

The height, *h*, of the triangle in Figure 4.23, can be calculated as

$$h = \mathrm{x}\sin\theta_z \tag{4.19}$$

Or as

$$h = \mathrm{z}\sin\theta_x \tag{4.20}$$

Also, the angles in that triangle can be calculated from its sides applying the law of cosines:

$$\begin{aligned}\cos\theta_x &= \frac{y^2+z^2-x^2}{2yz}\\ \cos\theta_y &= \frac{x^2+z^2-y^2}{2xz}\\ \cos\theta_z &= \frac{x^2+y^2-z^2}{2xy}\end{aligned} \tag{4.21}$$

Considering the law of cosines, (4.19) and (4.20), the height can be re-written as

$$h = \mathrm{x}\sin\left(\arccos\left(\frac{x^2+y^2-z^2}{2xy}\right)\right) \tag{4.22}$$

and

$$h = \mathrm{z}\sin\left(\arccos\left(\frac{y^2+z^2-x^2}{2yz}\right)\right) \tag{4.23}$$

So, the area of a generic triangle *x*-*y*-*z* can be calculated as:

$$\begin{aligned}A &= \frac{1}{2}\,x\,\mathrm{y}\sin\left(\arccos\left(\frac{x^2+y^2-z^2}{2xy}\right)\right)\\ A &= \frac{1}{2}\,y\,\mathrm{z}\sin\left(\arccos\left(\frac{y^2+z^2-x^2}{2yz}\right)\right)\\ A &= \frac{1}{2}\,z\,x\sin\left(\arccos\left(\frac{z^2+x^2-y^2}{2zx}\right)\right)\end{aligned} \tag{4.24}$$

And equation (4.15) can be transformed into:

$$V_{max} = \sqrt{\frac{{a_{max}}^2+{b_{max}}^2+{c_{max}}^2+4\sqrt{3}\,\frac{1}{2}\,b_{max}c_{max}\sin\left(\arccos\left(\frac{{b_{max}}^2+{c_{max}}^2-{a_{max}}^2}{2b_{max}c_{max}}\right)\right)}{2}} \tag{4.25}$$

Both equations (4.15) and (4.25) can be used to calculate the maximum phase-to-phase voltage with the available cells. As the method consists on calculate the parameters of a triangle, of course the following inequalities must be satisfied:

$$\begin{aligned}a_{max}+b_{max} &\geq c_{max}\\ b_{max}+c_{max} &\geq a_{max}\end{aligned} \tag{4.26}$$

$$c_{max} + a_{max} \geq b_{max}$$

If not, this balancing method cannot be applied.

Once the maximum balanced phase-to-phase voltage available is known, the voltage amplitude that each phase should supply is calculated. To do it the maximum voltage that each branch can reach with the available cells is considered. The calculations are done trying to have the phase-to-neutral voltages as equal as possible. The flux-diagram in Figure 4.24 summarizes the mentioned process, where *a*, *b*, and *c* are the amplitudes of vectors $\boldsymbol{V_A}$, $\boldsymbol{V_B}$, and $\boldsymbol{V_C}$, or what is the same, the value of phase-to-neutral voltages of each phase.

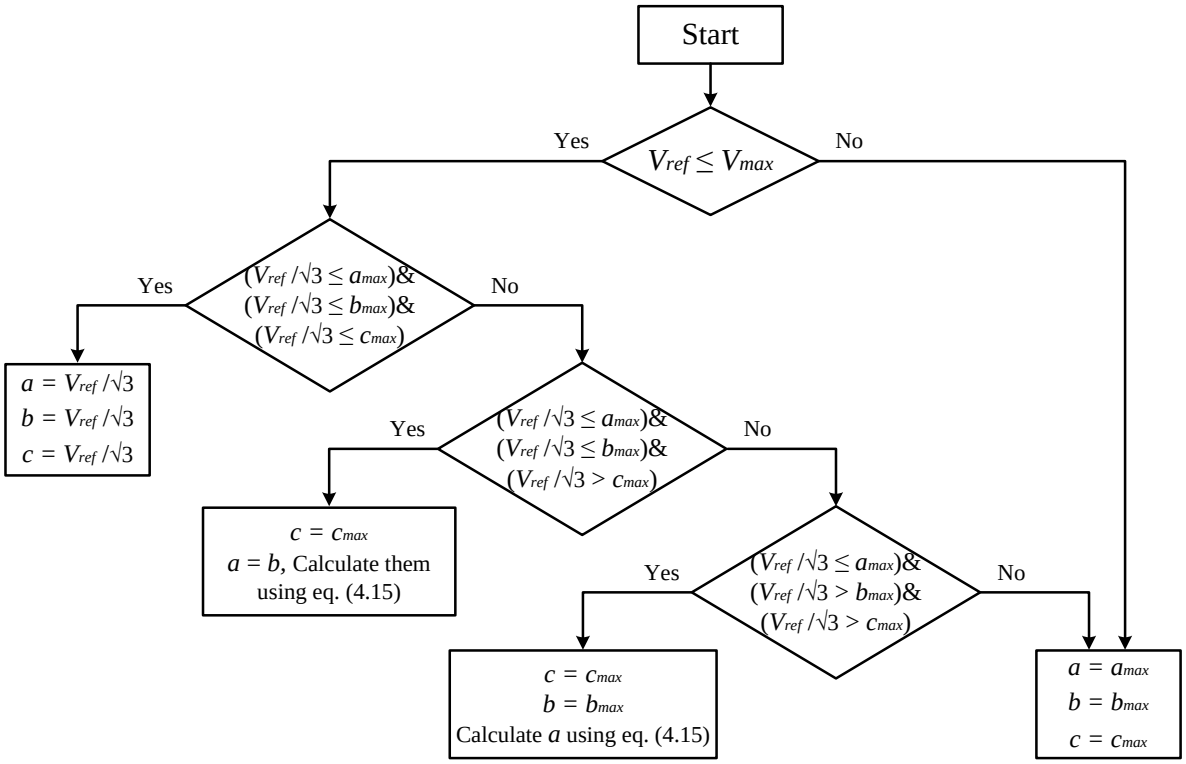


Figure 4.24. Flux-diagram of the neutral-shift calculation process.

The flux-diagram in Figure 4.24 summarizes the process considering the case in which $a_{max} \geq b_{max} \geq c_{max}$. Otherwise an analogue process must be followed.

Once the amplitudes of vectors $\boldsymbol{V_A}$, $\boldsymbol{V_B}$, and $\boldsymbol{V_C}$ are calculated, it is necessary to know their phases: φ_A, φ_B, and φ_C. In a balanced system the values for these parameters are

$$\begin{aligned} \varphi_A &= 0 \\ \varphi_B &= 4\pi/3 \\ \varphi_C &= 2\pi/3 \end{aligned} \tag{4.27}$$

But in this case, as the neutral point is shifted, it is necessary to recalculate those angles. This calculation is done considering the nomenclature used in Figure 4.21:

$$\begin{aligned} \varphi_A &= -(\alpha_A - \pi/6) \\ \varphi_B &= 4\pi/3 - (\beta_B - \pi/6) \\ \varphi_C &= 2\pi/3 - (\gamma_C - \pi/6) \end{aligned} \tag{4.28}$$

To calculate α_A, β_B, and γ_C, the law of the cosines is applied:

$$\begin{aligned} \alpha_A &= \cos^{-1}\frac{b^2 - {V_{ref}}^2 - a^2}{-2aV_{ref}} \\ \beta_B &= \cos^{-1}\frac{c^2 - {V_{ref}}^2 - b^2}{-2bV_{ref}} \\ \gamma_C &= \cos^{-1}\frac{a^2 - {V_{ref}}^2 - c^2}{-2cV_{ref}} \end{aligned} \tag{4.29}$$

Having the amplitudes *a*, *b*, and *c*, and phases φ_A, φ_B, and φ_C of the vectors, the phase-to-neutral voltage references are calculated as follows:

$$\begin{aligned} V_{refA} &= a \cdot \sin(\omega + \varphi_A) \\ V_{refB} &= b \cdot \sin(\omega + \varphi_B) \\ V_{refC} &= c \cdot \sin(\omega + \varphi_C) \end{aligned} \tag{4.30}$$

Table 4.3 indicates the available phase-to-phase output voltage applying this balancing method to CHB converters with a different number of cells.

4.3.5. Comparison between the explained balancing methods

In this subsection the intention is to compare the maximum balanced phase-to-phase voltage that can be obtained with the application of the methods explained in the previous subsections. Specifically the comparison includes the voltages that can be obtained through the bypassing of the cells in the same level (explained in subsection 4.3.1), using the SVM with redundant switching states (explained in subsection 4.3.2), and applying the neutral-shift method proposed in this Thesis (explained in subsection 4.3.4). The comparison is done for different number of faulty cells and for CHB converters with a number of cells from 2 to 8.

According to that, Figure 4.25 shows the comparison between maximum phase-to-phase voltages obtained when the previously explained balancing methods are used. Also the comparison is quantified in Table 4.4.

Table 4.3. Available phase-to-phase output voltage for the CHB converter depending on the number of faulty cells, for converters with 2, 3, 4, 5, 6, 7 and 8 cells per phase, when neutral-shift balancing method is used.

Available cells in phase A	Available cells in phase B	Available cells in phase C	Available output voltage (% V_{max})
Number of cells per phase = 2			
2	2	2	100
2	2	1	80.9
2	2	0	57.74
2	1	1	50
2	1	0	0
2	0	0	0
Number of cells per phase = 3			
3	3	3	100
3	3	2	87.77
3	3	1	73.59
3	3	0	57.74
3	2	2	75.46
3	2	1	50.92
3	2	0	0
3	1	1	0
3	1	0	0
3	0	0	0
Number of cells per phase = 4			
4	4	4	100
4	4	3	91.02
4	4	2	80.9
4	4	1	69.78
4	4	0	57.74
4	3	3	82.27
4	3	2	71.53
4	3	1	52.04
4	3	0	0
4	2	2	50
4	2	1	0
4	2	0	0
4	1	1	0
4	1	0	0
4	0	0	0
Number of cells per phase = 5			
5	5	5	100
5	5	4	92.92
5	5	3	85.08
5	5	2	76.57
5	5	1	67.45
5	5	0	57.74
5	4	4	86.06
5	4	3	78.13
5	4	2	68.96
5	4	1	52.92
5	4	0	0
Number of cells per phase = 7			
7	7	7	100
7	7	6	95.02
7	7	5	89.64
7	7	4	83.9
7	7	3	77.82
7	7	2	71.43
7	7	1	64.73
7	7	0	57.74
7	6	6	90.2
7	6	5	84.88
7	6	4	79.11
7	6	3	72.84
7	6	2	65.86
7	6	1	54.08
7	6	0	0
7	5	5	79.45
7	5	4	73.28
7	5	3	65.98
7	5	2	51.51
7	5	1	0
7	5	0	0
7	4	4	65.97
7	4	3	50.17
7	4	2	0
7	4	1	0
7	4	0	0
7	3	3	0
7	3	2	0
7	3	1	0
7	3	0	0
7	2	2	0
7	2	1	0
7	2	0	0
7	1	1	0
7	1	0	0
7	0	0	0
Number of cells per phase = 8			
8	8	8	100
8	8	7	95.67
8	8	6	91.02
8	8	5	86.09
8	8	4	80.9
8	8	3	75.46
8	8	2	69.78
8	8	1	63.87

Available cells in phase A	**Available cells in phase B**	**Available cells in phase C**	**Available output voltage (% V_{max})**	**Available cells in phase A**	**Available cells in phase B**	**Available cells in phase C**	**Available output voltage (% V_{max})**
5	3	3	69.15	8	8	0	57.74
5	3	2	50.33	8	7	7	91.46
5	3	1	0	8	7	6	68.88
5	3	0	0	8	7	5	81.97
5	2	2	0	8	7	4	76.71
5	2	1	0	8	7	3	71.08
5	2	0	0	8	7	2	64.87
5	1	1	0	8	7	1	54.49
5	1	0	0	8	7	0	0
5	0	0	0	8	6	6	82.27
Number of cells per phase = 6				8	6	5	77.19
6	6	6	100	8	6	4	71.53
6	6	5	94.15	8	6	3	64.94
6	6	4	87.77	8	6	2	52.04
6	6	3	80.9	8	6	1	0
6	6	2	73.59	8	6	0	0
6	6	1	65.87	8	5	5	71.65
6	6	0	57.74	8	5	4	64.89
6	5	5	88.49	8	5	3	50.52
6	5	4	82.14	8	5	2	0
6	5	3	75.11	8	5	1	0
6	5	2	67.17	8	5	0	0
6	5	1	53.58	8	4	4	50
6	5	0	0	8	4	3	0
6	4	4	75.46	8	4	2	0
6	4	3	67.34	8	4	1	0
6	4	2	50.92	8	4	0	0
6	4	1	0	8	3	3	0
6	4	0	0	8	3	2	0
6	3	3	50	8	3	1	0
6	3	2	0	8	3	0	0
6	3	1	0	8	2	2	0
6	3	0	0	8	2	1	0
6	2	2	0	8	2	0	0
6	2	1	0	8	1	1	0
6	2	0	0	8	1	0	0
6	1	1	0	8	0	0	0
6	1	0	0				
6	0	0	0				

From Figure 4.25 and Table 4.4, it is observed that when the cells in the same level are bypassed the available balanced voltage decreases faster than when space vector modulation or the neutral shift methods are used. For this reason it is advisable not use this method to balance the phase-to-phase voltage. On the other hand, as it was said previously, using the redundant states in space vector modulation can be very complex in high number of levels converters. So, in this case it is recommended to use the neutral shift method.

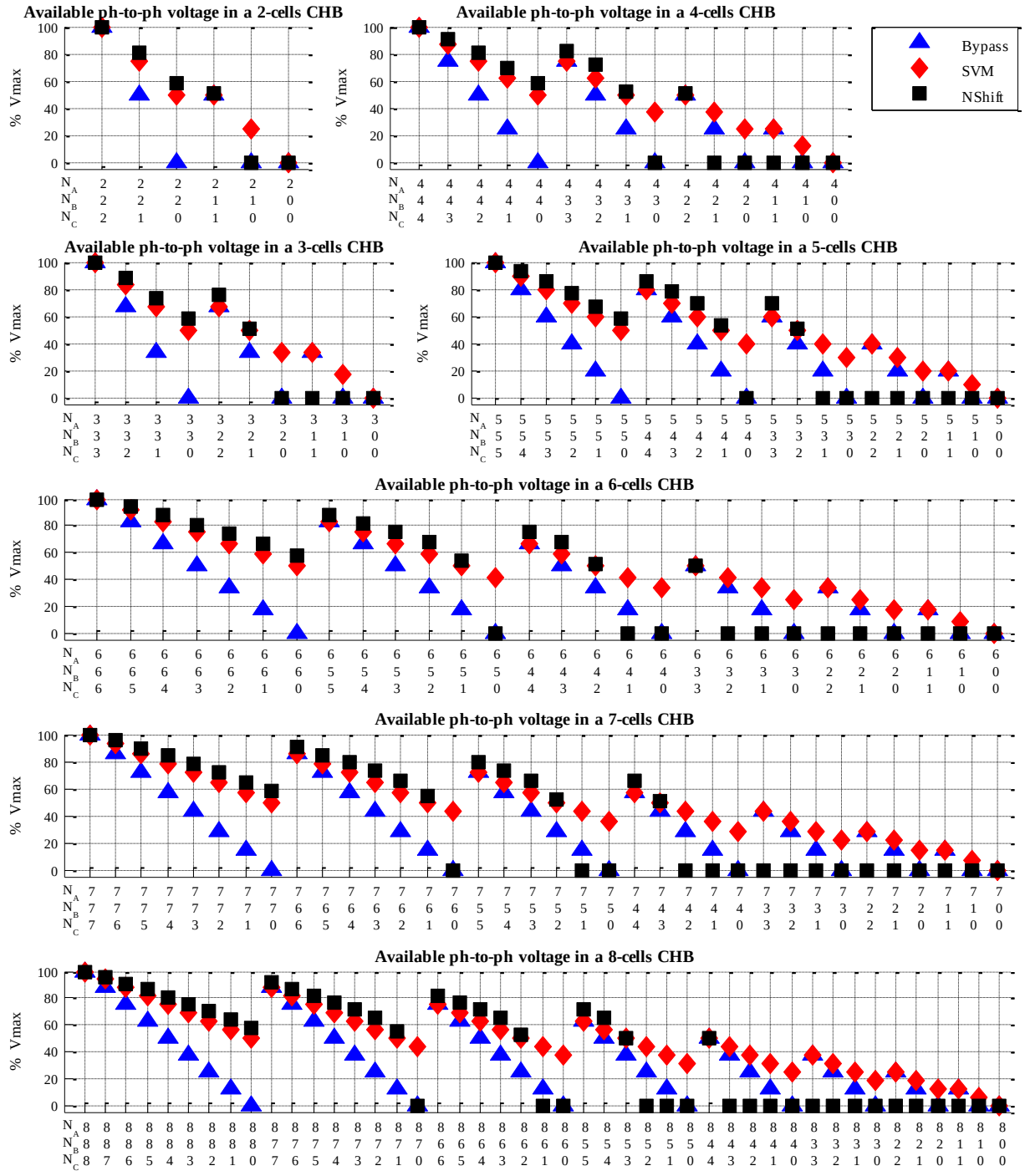


Figure 4.25. Available balanced phase-to-phase voltage with the application of the different balancing methods, for CHB converters of 2, 3, 4, 5, 6, 7, and 8 cells per phase. In each graph N_A, N_B, and N_C represent the number of available (non-faulty) cells in the corresponding phase.

Table 4.4. Comparison of the available phase-to-phase output voltage for the CHB converter depending on the number of available cells (N_A, N_B, and N_C), for converters with 2, 3, 4, 5, 6, 7 and 8 cells per phase, when the explained methods are used: bypassing the cells in the same level, using the redundant states of SVM, and applying neutral-shift.

N_A	N_B	N_C	Voltage (%) bypassing	Voltage (%) SVM	Voltage (%) NS
Number of cells per phase = 2					
2	2	2	100	100	100
2	2	1	50	75	80.9
2	2	0	0	50	57.74
2	1	1	50	50	50
2	1	0	0	25	0
2	0	0	0	0	0
Number of cells per phase = 3					
3	3	3	100	100	100
3	3	2	66.67	83.33	87.77
3	3	1	33.33	66.67	73.59
3	3	0	0	50	57.74
3	2	2	66.67	66.67	75.46
3	2	1	33.33	50	50.92
3	2	0	0	33.33	0
3	1	1	33.33	33.33	0
3	1	0	0	16.67	0
3	0	0	0	0	0
Number of cells per phase = 4					
4	4	4	100	100	100
4	4	3	75	87.5	91.02
4	4	2	50	75	80.9
4	4	1	25	62.5	69.78
4	4	0	0	50	57.74
4	3	3	75	75	82.27
4	3	2	50	62.5	71.53
4	3	1	25	50	52.04
4	3	0	0	37.5	0
4	2	2	50	50	50
4	2	1	25	37.5	0
4	2	0	0	25	0
4	1	1	25	25	0
4	1	0	0	12.5	0
4	0	0	0	0	0
Number of cells per phase = 5					
5	5	5	100	100	100
5	5	4	80	90	92.92
5	5	3	60	80	85.08
5	5	2	40	70	76.57
5	5	1	20	60	67.45
5	5	0	0	50	57.74
5	4	4	80	80	86.06
5	4	3	60	70	78.13
5	4	2	40	60	68.96
5	4	1	20	50	52.92
5	4	0	0	40	0
5	3	3	60	60	69.15
5	3	2	40	50	50.33
Number of cells per phase = 7					
7	7	7	100	100	100
7	7	6	85.71	92.86	95.02
7	7	5	71.43	85.71	89.64
7	7	4	57.14	78.57	83.9
7	7	3	42.86	71.43	77.82
7	7	2	28.57	64.29	71.43
7	7	1	14.29	57.14	64.73
7	7	0	0	50	57.74
7	6	6	85.71	85.71	90.2
7	6	5	71.43	78.57	84.88
7	6	4	57.14	71.43	79.11
7	6	3	42.86	64.29	72.84
7	6	2	28.57	57.14	65.86
7	6	1	14.29	50	54.08
7	6	0	0	42.86	0
7	5	5	71.43	71.43	79.45
7	5	4	57.14	64.29	73.28
7	5	3	42.86	57.14	65.98
7	5	2	28.57	50	51.51
7	5	1	14.29	42.86	0
7	5	0	0	35.71	0
7	4	4	57.14	57.14	65.97
7	4	3	42.86	50	50.17
7	4	2	28.57	42.86	0
7	4	1	14.29	35.71	0
7	4	0	0	28.57	0
7	3	3	42.86	42.86	0
7	3	2	28.57	35.71	0
7	3	1	14.29	28.57	0
7	3	0	0	21.43	0
7	2	2	28.57	28.57	0
7	2	1	14.29	21.43	0
7	2	0	0	14.29	0
7	1	1	14.29	14.29	0
7	1	0	0	7.14	0
7	0	0	0	0	0
Number of cells per phase = 8					
8	8	8	100	100	100
8	8	7	87.5	93.75	95.67
8	8	6	75	87.5	91.02
8	8	5	62.5	81.25	86.09
8	8	4	50	75	80.9
8	8	3	37.5	68.75	75.46
8	8	2	25	62.5	69.78
8	8	1	12.5	56.25	63.87
8	8	0	0	50	57.74
8	7	7	87.5	87.5	91.46

N_A	N_B	N_C	Voltage (%) bypassing	Voltage (%) SVM	Voltage (%) NS
5	3	1	20	40	0
5	3	0	0	30	0
5	2	2	40	40	0
5	2	1	20	30	0
5	2	0	0	20	0
5	1	1	20	20	0
5	1	0	0	10	0
5	0	0	0	0	0
Number of cells per phase = 6					
6	6	6	100	100	100
6	6	5	83.33	91.67	94.15
6	6	4	66.67	83.33	87.77
6	6	3	50	75	80.9
6	6	2	33.33	66.67	73.59
6	6	1	16.67	58.33	65.87
6	6	0	0	50	57.74
6	5	5	83.33	83.33	88.49
6	5	4	66.67	75	82.14
6	5	3	50	66.67	75.11
6	5	2	33.33	58.33	67.17
6	5	1	16.67	50	53.58
6	5	0	0	41.67	0
6	4	4	66.67	66.67	75.46
6	4	3	50	58.33	67.34
6	4	2	33.33	50	50.92
6	4	1	16.67	41.67	0
6	4	0	0	33.33	0
6	3	3	50	50	50
6	3	2	33.33	41.67	0
6	3	1	16.67	33.33	0
6	3	0	0	25	0
6	2	2	33.33	33.33	0
6	2	1	16.67	25	0
6	2	0	0	16.67	0
6	1	1	16.67	16.67	0
6	1	0	0	8.33	0
6	0	0	0	0	0
8	7	6	75	81.25	68.88
8	7	5	62.5	75	81.97
8	7	4	50	68.75	76.71
8	7	3	37.5	62.5	71.08
8	7	2	25	56.25	64.87
8	7	1	12.5	50	54.49
8	7	0	0	43.75	0
8	6	6	75	75	82.27
8	6	5	62.5	68.75	77.19
8	6	4	50	62.5	71.53
8	6	3	37.5	56.25	64.94
8	6	2	25	50	52.04
8	6	1	12.5	43.75	0
8	6	0	0	37.5	0
8	5	5	62.5	62.5	71.65
8	5	4	50	56.25	64.89
8	5	3	37.5	50	50.52
8	5	2	25	43.75	0
8	5	1	12.5	37.5	0
8	5	0	0	31.25	0
8	4	4	50	50	50
8	4	3	37.5	43.75	0
8	4	2	25	37.5	0
8	4	1	12.5	31.25	0
8	4	0	0	25	0
8	3	3	37.5	37.5	0
8	3	2	25	31.25	0
8	3	1	12.5	25	0
8	3	0	0	18.75	0
8	2	2	25	25	0
8	2	1	12.5	18.75	0
8	2	0	0	12.5	0
8	1	1	12.5	12.5	0
8	1	0	0	6.25	0
8	0	0	0	0	0

4.4. Applications for CHB converters

The CHB topology was conceived principally for its use in medium voltage and high power drives [87] (for high range of voltage, i.e. from 6.6 kV, CHB is in practice the only solution), as one of its main advantages is the modularity, and because it can be configured as a fault-tolerant topology, as it has been shown in the previous section. But this topology has two main disadvantages:

- The necessity of an exhaustive design for the multi-pulse transformer, in such way that for all the secondary windings the leakage inductance be the same.

- High common-mode voltages are generated in the cells, especially in those that are further from the neutral point. This point is out of the scope of this Thesis.

Even though its main application is as induction motor drives, the cascaded H-bridge converter has been used in other applications connected to the grid, and even for renewable energy resources integration [88], [89].

4.4.1. Drive applications

As was mention, there are multiple examples of using the cascaded H-bridge converter for induction motor drives, whether for industrial applications [90]-[92] or automotive applications [93]-[94]. The operation and control basis of induction motors is explained in Appendix C, and whatever the application, the basic scheme for a drive based in CHB converter is shown in Figure 4.26. This application based on CHB topology will be studied in depth later in this work.

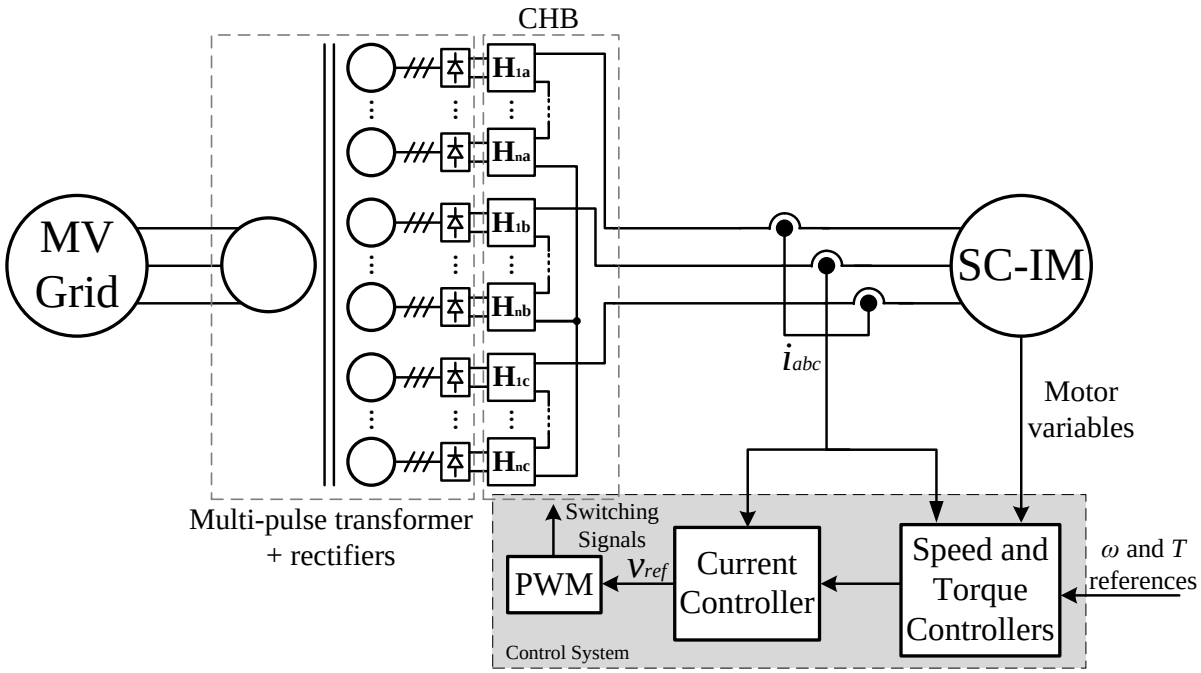


Figure 4.26. Basic scheme of an induction motor drive based on CHB converter.

4.4.2. Power quality applications

There are many examples of the use of CHB converters in flexible AC transmission systems (FACTS), like [95]-[96]. Probably one of the most used FACTS applications is the static compensator (STATCOM) system. There are also some examples in technical literature of the use of CHB in STATCOMs [97]-[99]. This application is illustrated in Figure 4.27 and will be studied in detail later.

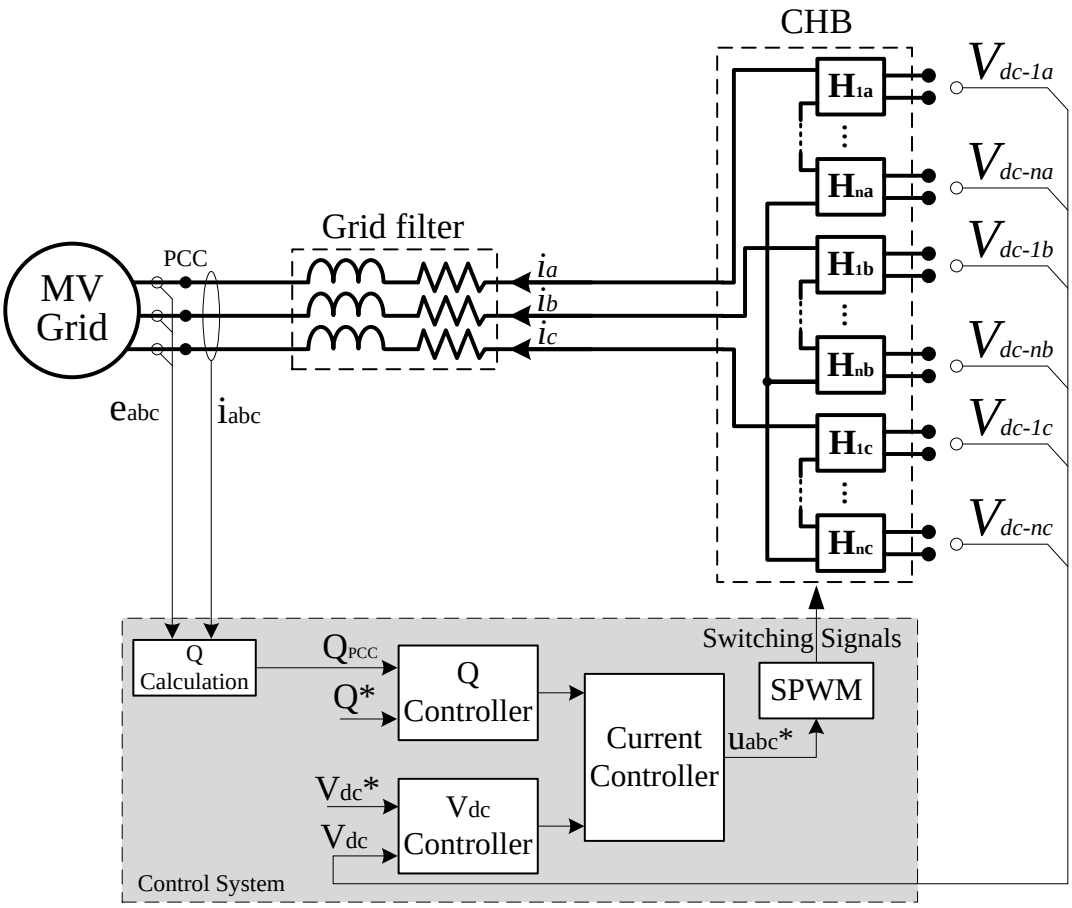


Figure 4.27. Illustration of CHB converter used for a STATCOM system.

4.4.3. Peculiarities of CHB converters control

There are some considerations that should be having into account when the CHB is used. One of them is the voltage value considered to do the voltage references normalization before apply the desired modulation method. As in this converter there is not a single DC supply, but there are as many supplies as cells in the converter, the normalization process is done separately for each phase using the sum of the DC voltages of the cells in it. What means that the voltage reference for a phase is divided by the sum of its cells DC voltages before the modulation method is applied. The sum of the cells DC voltages in a phase can be considered as the equivalent DC voltage for this phase. This process is illustrated in the block diagram of Figure 4.28.

The other main consideration to have into account is when the CHB is included in a power quality application such as a STATCOM. In this case, the input value for the DC voltage controller should be the average of equivalent DC voltage of the three phases. For better understanding of this process Figure 4.29 includes its block diagram.

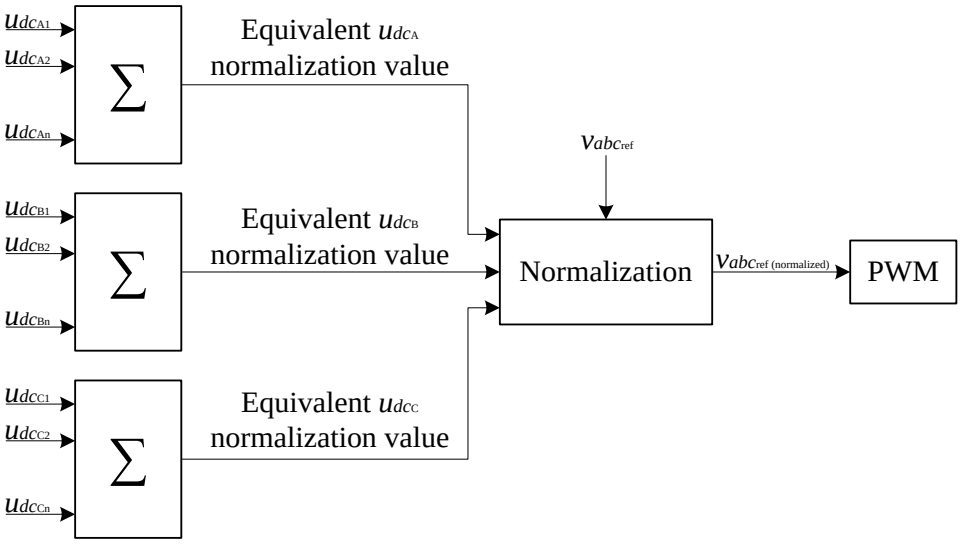


Figure 4.28. Block diagram for the voltage references normalization process in the CHB converter.

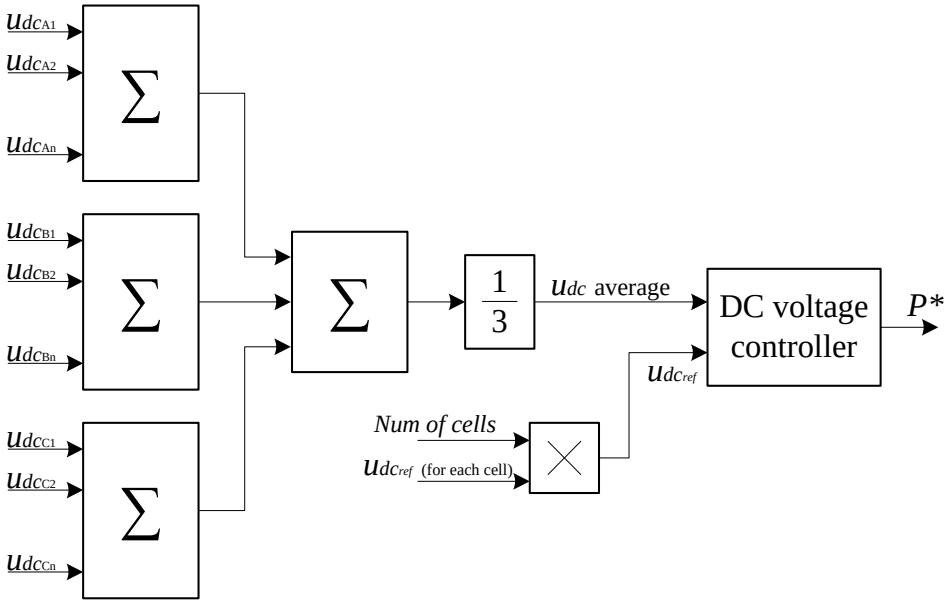


Figure 4.29. Block diagram of the DC voltage reference calculation for the DC voltage controller in a CHB converter.

Chapter 5: MODULAR MULTILEVEL CONVERTER

This chapter is about the topology known as Modular Multilevel Converter (MMC). This name makes reference to those converters that are composed by some submodules series-connected that share the same voltage source. Those submodules can have different structures, and their operation will depend on this factor. In the following subsections this topology is studied as well as its usual modulation methods and its industrial applications.

As in the case of the cascaded H-bridge converter, the MMC has the advantage of its modularity, which can be very useful in case of fault in a device. This characteristic of the topology will be also studied in this chapter.

5.1. Topology description

As it was mention in chapter 2, Modular Multilevel Converter (MMC) topology is composed by some submodules connected in series per branch. This series connection remembers the cascade H-bridge topology, but with the difference that in this case all submodules share the DC source instead of having an isolated DC supply for each one. With this peculiarity, the general aspect for a three-phase MMC converter was shown in Figure 2.6, and it is reproduced again here in Figure 5.1. As it was mentioned, in each branch there are n submodules that are spread evenly in two arms: the upper and the lower, and this condition can be achieved only if n is an even integer. Both arms are connected together through two arm inductors named L_{MMC}. As in the case of CHB, the number of submodules that a MMC has in each of its phases and their type determine the number of levels in the converter output voltage. In this way, a MMC with n 2-level submodules per phase will have $n/2 + 1$ or $n + 1$ levels in its output voltage depending on the modulation strategy (this point will be studied further ahead).

The kind of submodule chosen for the modular multilevel converter will determine the operation and the way of modulation. The submodules that compose a MMC can be of multiple configurations. The most used are the half-bridge and the full-bridge submodules (Figure 5.2), but there are more that can be used: NPC submodule, flying capacitor submodule, etc. [100]-[102]. In this work the submodule used is the half-bridge submodule (Figure 5.2.a) that is composed by two devices known as top and bottom, or S and $\bar{S}$; all the modulation methods explained and the examples shown are obtained using this type of submodule. According to this, and using the nomenclature that appears in Figure 5.1, the general expression for the phase-to-neutral voltage in a MMC with n submodules per branch can be calculated from:

$$v_{XN} = {}^{1}/_{2}\left[\left(v_{SM\,X\left(\frac{n}{2}+1\right)} + \cdots + v_{SM\,Xn}\right) - \left(v_{SM\,X1} + \cdots + v_{SM\,X\left(\frac{n}{2}\right)}\right)\right] \tag{5.1}$$

where $X = A$, B, or C.

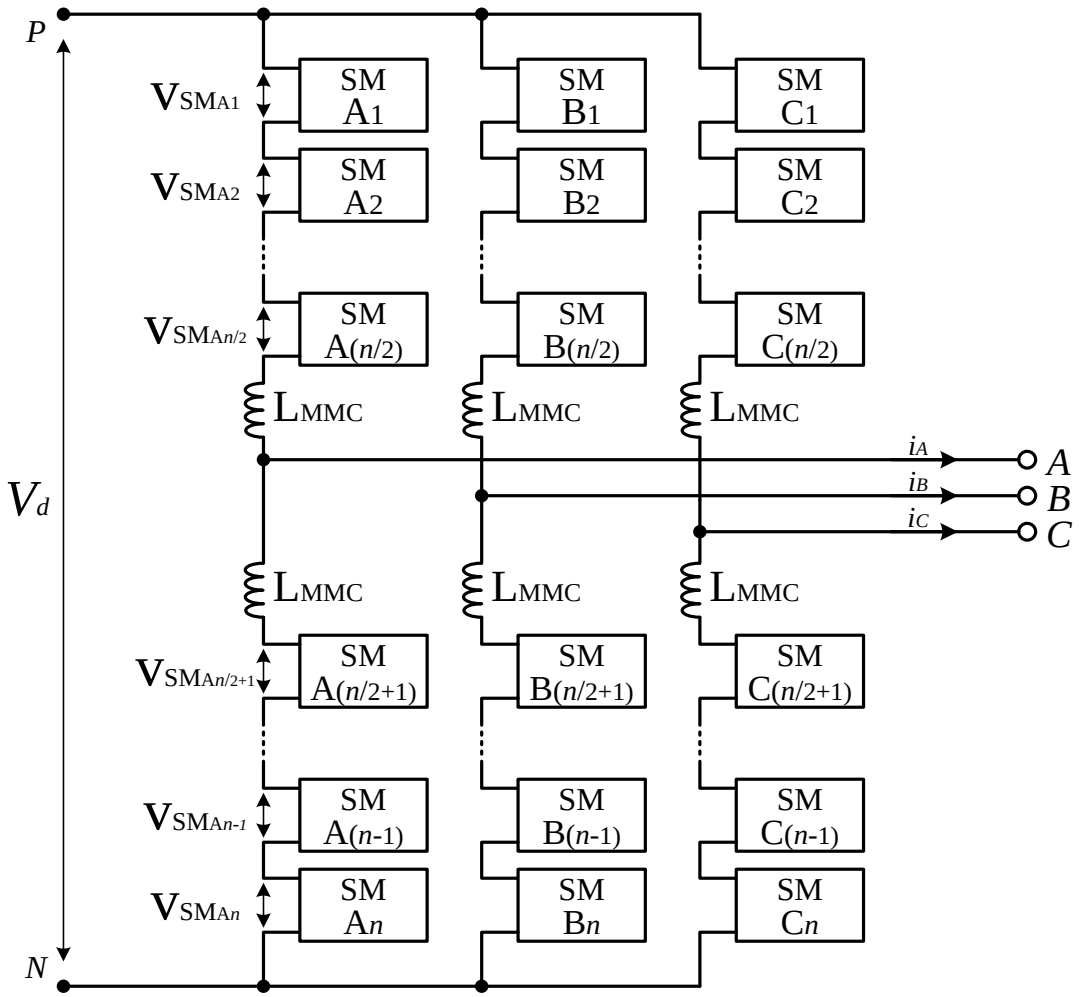
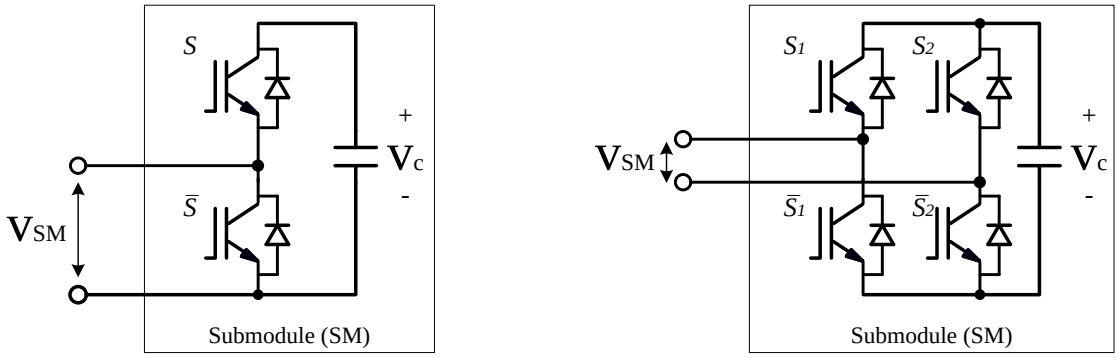


Figure 5.1. General representation of Modular Multilevel converter.



a) b)

Figure 5.2. Examples of half-bridge submodule a), and full-bridge submodule b).

From Figure 5.1 and Figure 5.2.a) the reader can see that the output voltage of a generic submodule, SM_k, depends on the state of the power devices that compose it (S_k, and $\bar{S}_k$). In such way, as the behavior of $\bar{S}_k$ is complementary to S_k, the output voltage of a submodule can be determined as:

$$v_{SMk} = v_{ck} \cdot S_k \tag{5.2}$$

The DC voltage, v_{DC}, is shared among the submodules in each branch. The voltage distribution between the submodules depends on the used modulation strategy. In technical literature there are two strategies well defined that are known as *N+1* and *2N+1*, being N the number of submodules in an arm, or what is the same $N = n/2$ [103]-[104]. In the strategy *2N+1* each arm is modulated independently, and the output voltage depends on the number of submodules connected in both arms, the upper and the lower. With this strategy the maximum number of voltage levels in the output is 2*N*+1. The disadvantage of this strategy is that as the number of submodules activated at the same time is not constant, large submodules voltage unbalances are generated, especially in the case of MMC with low number of submodules [105].

However in the strategy *N+1* the submodules are modulated in such way that the number of activated submodules is always constant. This is done commutating inversely the upper and lower arms of each phase. Despite this strategy generates less output levels (*N*+1 as maximum), as the number of active submodules is constant, the capacitors voltage oscillations are reduced.

In this work it is used the strategy *N+1*, so, as the number of active submodules is constant every time, the voltage of each submodule, v_c, is calculated in the following way:

$$v_c = \frac{v_{DC}}{n/2} \tag{5.3}$$

As it was mentioned, the upper and lower arms are commutated inversely; this is achieved making the submodules behavior on the upper arm complementary one by one with those of the lower arm. For example, $S_{n/2+1}$ complementary to S_1, $S_{n/+2}$ complementary to S_2, etc. In this way, the voltage in the upper arm, v_u, and the lower arm, v_l, can be calculated from the following expressions:

$$v_u = \sum_{k=1}^{n/2} v_{ck} \cdot (1 - S_k) \tag{5.4}$$

$$v_l = \sum_{k=n/2+1}^{n} v_{ck} \cdot S_k \tag{5.5}$$

And the phase-to-neutral voltage comes from the equation

$$v_{ph-N} = \frac{v_l - v_u}{2} \tag{5.6}$$

what is equivalent to equation (5.1).

Following the strategy chosen in this case, in the next section the most used techniques to modulate this kind of converters will be explained.

Moreover, this topology has some peculiarities that must been considered. On one hand, due to the proper connection of the submodules in this topology, circulating currents are generated, and in order to avoid extra losses, these currents must to be cancelled. This issue is out of the scope of this thesis and because of that it is not explained in this work, but is well explained in the work [106], in which this author has collaborated.

On the other hand, for the right operation of the converter, the voltage in all the submodules must be as most equal as possible; for this reason it is advisable to implement a method for balancing the capacitors voltage. This issue is related to the modulation of the converter and, hence will be treated in the next subsection.

5.2. Modulation methods

5.2.1. Pulse-Width Modulation for modular multilevel converters

As was explained in the previous chapter, sinusoidal PWM (SPWM) is one of the most used modulation techniques for multilevel converters, and hence for MMCs. In the same way that for other kind of converters, in the case of the MMC, the SPWM is based in the comparison of a modulation signal with one or more carrier signals, and the result of that comparison is obtaining the firing signals for the devices that compose the submodules.

According to that, for a half-bridge submodule like the one depicted in Figure 5.2.a), the firing signal for the top device, S, and the bottom device, $\bar{S}$, will be determined as follows:

$$S = \begin{cases} On & if \quad v_m \geq v_{cr} \\ Off & if \quad v_m < v_{cr} \end{cases}$$
$$\bar{S} = \begin{cases} Off & if \quad v_m \geq v_{cr} \\ On & if \quad v_m < v_{cr} \end{cases} \tag{5.7}$$

where v_m represents the modulation signal, and v_{cr} stands for the carrier signal corresponding to this submodule.

Figure 5.3 shows a representation of SPWM signals for a half-bridge submodule and the resultant harmonic content for the submodule output voltage, v_{SM}. Note that in the harmonic content there is a hard continuous component, due to the output voltage oscillates between 0 and v_c, and the principal band of harmonics are sited around the m_f^{th} harmonic and its multiples. This harmonic disposition is similar to the obtained when a full-H-bridge is modulated with bipolar approach (Figure 4.5) except for the DC component.

Figure 5.4 shows the evolution of the harmonics that compose the four firsts bands as the amplitude modulation index, m_a, grows. In this figure it can be proved that the effect of DC component is very hard due to we are studying the output voltage of a single submodule. If the output voltage of a whole arm is studied, the DC component disappears as can be seen in Figure 5.5.

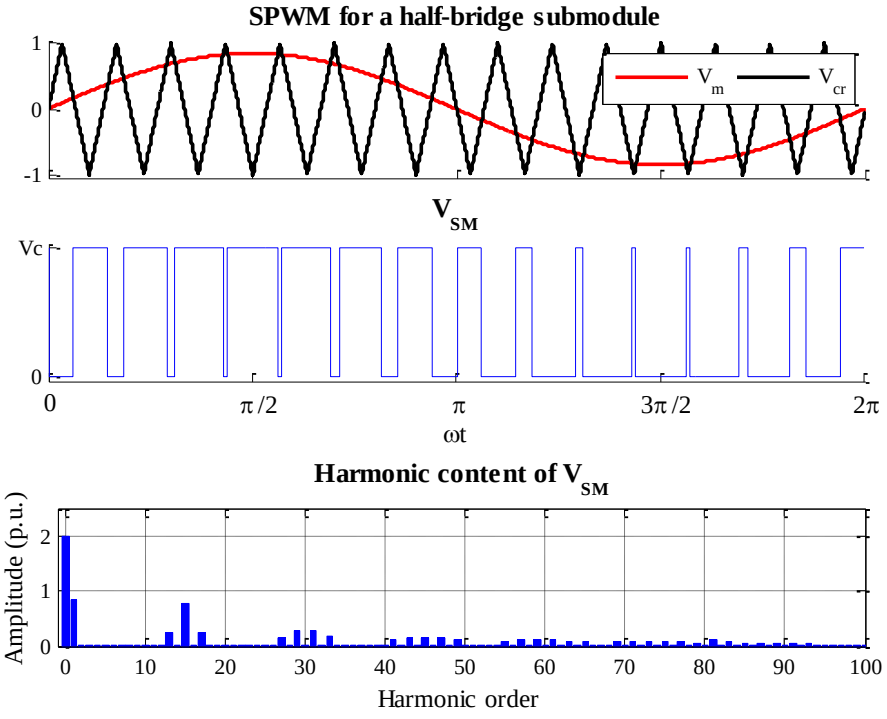


Figure 5.3. Representation of the SPWM signals for a half-bridge submodule, and harmonic content of the output voltage obtained (f_m = 50 Hz, f_{cr} = 750 Hz, m_f = 15, m_a = 0.85).

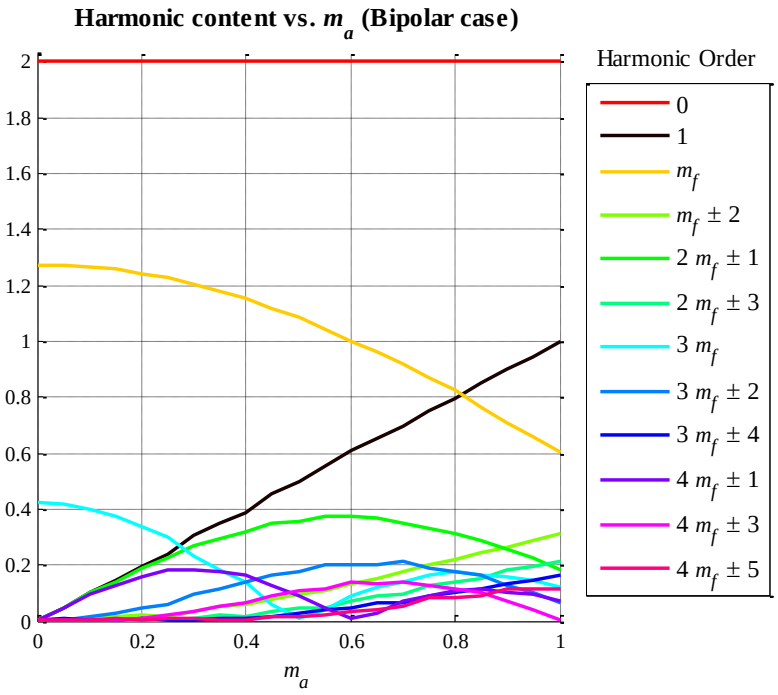


Figure 5.4. Harmonic content of the output voltage for a half-bridge submodule, as a function of the amplitude modulation index, m_a.

As it was mentioned previously, only the *N+1* strategy will be studied in this work. According to that, for the SPWM modulation scheme, in a MMC with five submodules per arm or, what is the same, ten per phase (N = 5, n = 10), it can be achieved a total of six levels in the output voltage ($n/2$ + 1, or N + 1). In those conditions, a carrier signal is needed for each submodule in an arm, in this case a total of five. The angle between carrier signals is calculated similarly to the CHB case:

$$\delta = \frac{2\pi}{Num\ of\ cells\ in\ an\ arm} \tag{5.8}$$

So, in this case, these carrier signals will have the same frequency and amplitude, and will be shifted an angle of 2π/5 radians one from each other. As it was explained earlier, the submodules of the lower arm have complementary behavior to those in the upper arm. Figure 5.5 shows an example of SPWM for a six-level MMC.

Figure 5.5 shows as the phase-to-neutral voltage has its main band of harmonics around the 75th harmonic, what is five times the carrier frequency (5 m_f), and the second band is around 150th harmonic, that is the double of the first band.

In general terms, the first band of harmonics in a MMC with N submodules per arm is sited around the harmonic number $N \cdot m_f$. According to that, for each pair of submodules that is

added in a phase (one in each arm), the main harmonics band of the phase-to-neutral voltage splits m_f harmonics to the right side.

The evolution of bands around the 75th and the 150th harmonics (first and second bands) has been analyzed, and the results are shown in Figure 5.6. As happened in the case of CHB, in this case it can be seen that the number of harmonics that compose the first and second bands is higher than in the case of a single half-bridge submodule, but their amplitudes are lower and their location is further from the fundamental harmonic. And also the DC component is eliminated as the output voltage is symmetrical respect to the zero level.

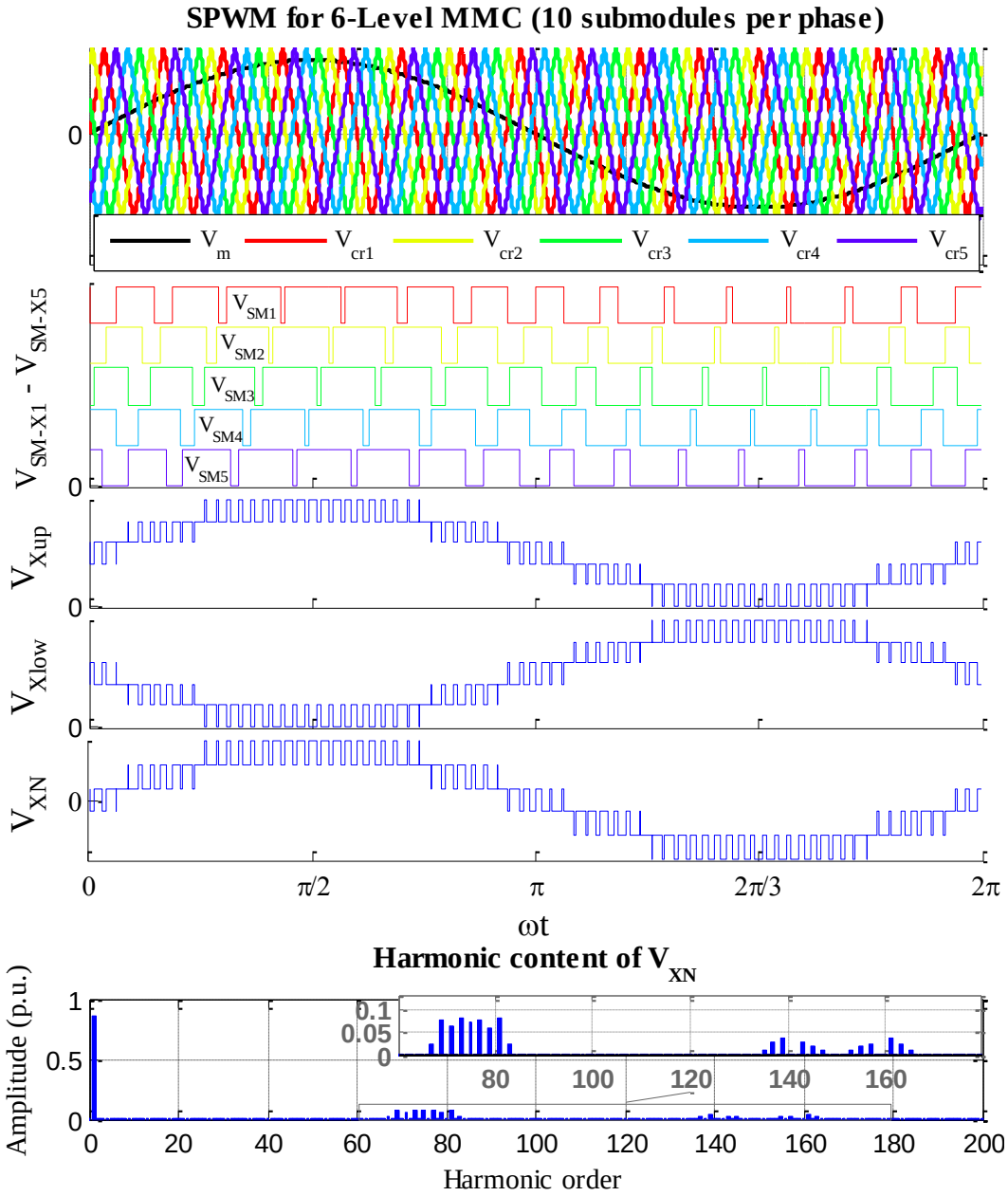


Figure 5.5. Example of SPWM scheme for a six-level MMC (f_m = 50 Hz, f_{cr} = 750 Hz, m_f = 15, m_a = 0.85), for a generic phase X (where X = A, B, or C).

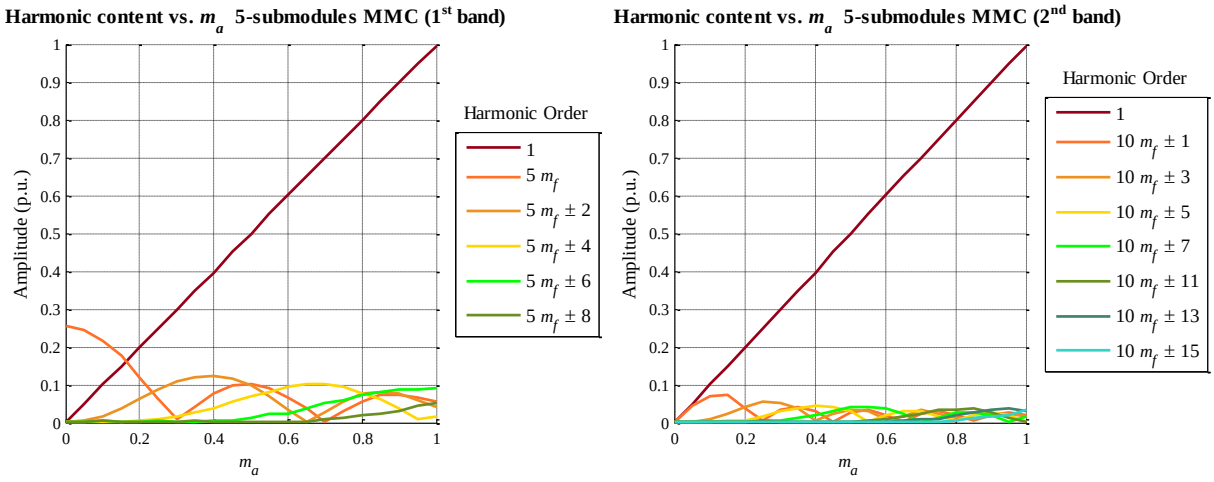


Figure 5.6. Evolution of first (around 75th) and second (around 150th) harmonic bands as a function of m_a.

5.2.2. Space vector modulation

As was mentioned in the previous chapter, the space vector modulation conveniently provides more flexibility to optimize switching waveforms due to the existence of redundant switching states and adjustable duty cycles, and it is suitable to be digitally implemented [73]. But the disadvantage comes when there is a high number of levels in the converter, in those cases the algorithm complexity grows. As was illustrated in section 4.2.2, if a converter has n voltage levels, there are n^3 switching states and $6\cdot(n\text{-}1)^2$ triangles in its corresponding space vector diagram [77].

Instead of handling a high number or space vectors and switching states, there are methods based on the SVM that simplify the complexity of this modulation. For example, in [79] is presented a method that avoids the use of coordinate transformations and allows its adaptation for any number of levels in the converter, n, with minimum modifications. This algorithm consists on find the four closest space vectors to the voltage reference vector, as is shown in the example of Figure 5.7. See as $V_{ab}{}^n$, $V_{bc}{}^n$, and $V_{ca}{}^n$, represent the normalized projections of V_{ref} over the axes *ab*, *bc*, and *ca*, respectively.

According to that, the closest vectors V_{ul}, V_{lu}, V_{uu}, and V_{ll}, are calculated through the upper and lower rounded integer values of $V_{ab}{}^n$ and $V_{bc}{}^n$ in the following way:

$$V_{ul} = \begin{bmatrix} \lceil V_{ab}^n \rceil \\ \lfloor V_{bc}^n \rfloor \end{bmatrix} \qquad V_{uu} = \begin{bmatrix} \lceil V_{ab}^n \rceil \\ \lceil V_{bc}^n \rceil \end{bmatrix}$$
$$V_{lu} = \begin{bmatrix} \lfloor V_{ab}^n \rfloor \\ \lceil V_{bc}^n \rceil \end{bmatrix} \qquad V_{ll} = \begin{bmatrix} \lfloor V_{ab}^n \rfloor \\ \lfloor V_{bc}^n \rfloor \end{bmatrix} \tag{5.9}$$

As it can be seen in Figure 5.7, V_{ul} and V_{lu} are always two of the three vectors that delimit the triangle where lays the reference vector. The third vector of that triangle is chosen following these rules:

$$\begin{cases} V_{uu} & if \quad V_{ca}^{n} + (\lceil V_{ab}^{n} \rceil + \lfloor V_{bc}^{n} \rfloor) < 0 \\ V_{ll} & if \quad V_{ca}^{n} + (\lceil V_{ab}^{n} \rceil + \lfloor V_{bc}^{n} \rfloor) > 0 \end{cases} \tag{5.10}$$

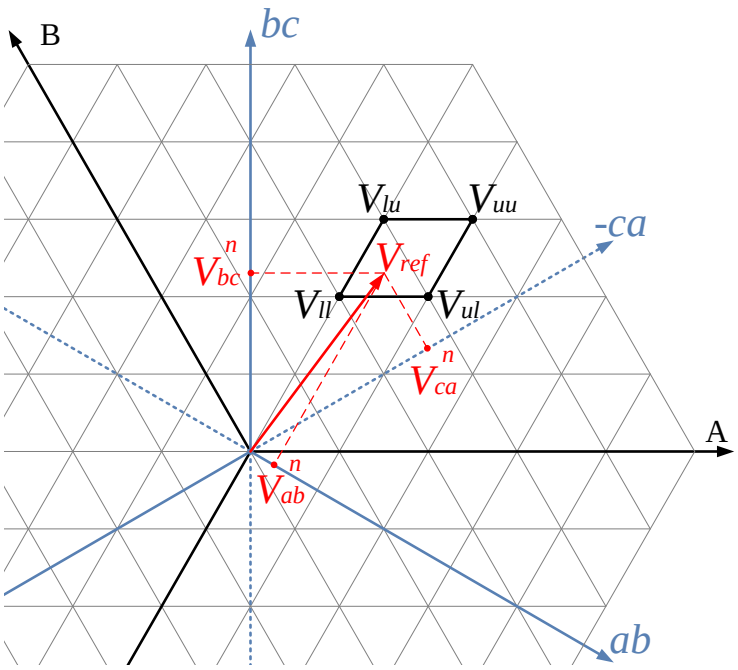


Figure 5.7. Example of the localization of the four closest space vectors to the reference, in a space vector diagram for a 6-level converter.

The way of calculating the duty cycles for these three vectors depends on whether the third vector is V_{uu} or V_{ll}. If V_{ll} the duty cycles are calculated as follows:

$$\begin{cases} d_{ul} = V_{ab}^{n} - \lfloor V_{ab}^{n} \rfloor \\ d_{lu} = V_{bc}^{n} - \lfloor V_{bc}^{n} \rfloor \\ d_{ll} = 1 - d_{ul} - d_{lu} \end{cases} \tag{5.11}$$

In the case of the third vector is V_{uu}, the duty cycles will be:

$$\begin{cases} d_{ul} = -(V_{bc}^{n} - \lceil V_{bc}^{n} \rceil) \\ d_{lu} = -(V_{ab}^{n} - \lceil V_{ab}^{n} \rceil) \\ d_{ll} = 1 - d_{ul} - d_{lu} \end{cases} \tag{5.12}$$

The switching states to be applied are selected after determining the available states for each vector. The selection is done through the following formula:

$$\begin{bmatrix} \mathrm{k} \\ \mathrm{k} - V(1) \\ \mathrm{k} - V(1) - V(2) \end{bmatrix} \tag{5.13}$$

where $k \in [0, n\text{-}1]$, and $V(1)$ and $V(2)$ are the *ab* and *bc* components respectively of the corresponding vector (V_{ul}, V_{lu}, V_{uu}, V_{ll}).

5.2.3. Nearest level modulation

Nearest level modulation is a modulation technique very interesting to apply to MMCs with large number of submodules. Considering that nowadays in industry there are MMCs of up to more than 200 submodules (for example, INELFE project [107] presents MMCs with 401 levels), this technique supposes a clear advantage over other modulation methods like SPWM or SVM: following with the same example, for modulate with SPWM a MMC with 800 submodules a total of 400 carrier signals would be necessary; and in the case of using SVM with a MMC like that, the number of switching states would be 401^3. As the reader can see, in a case like that the complexity of applying SPWM or SVM makes them unfeasible to use.

NLM is based on generating the reference voltage by using two different voltage levels. Applying each voltage level during a certain period of time is possible to generate a signal whose mean value is the desired value. The principle of operation of this method is explained in [108], and it is briefly illustrated in Figure 5.8, where V_N and V_{N-1} are respectively the voltages corresponding to a certain level, and the immediately lower level, V_{ref} is the desired voltage, d is the duty cycle, and T_{sw} is the period corresponding to the chosen switching frequency, f_{sw}.

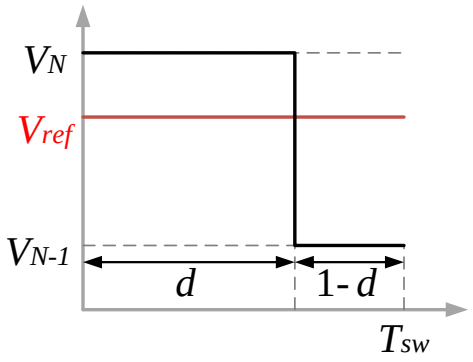


Figure 5.8. Illustration of the operation principle of Nearest Level Modulation.

Obviously, the total number of levels in which the output signal can be divided depends on the number of submodules in the MMC. The generalized formula for two generic consecutive levels (*N*-1 and *N*) is the following:

$$V_{ref} = V_N d + V_{N-1}(1 - d) \tag{5.14}$$

where the desired output, V_{ref}, is sited between the consecutive voltage levels V_N and V_{N-1}. The duty cycle (d) for each switching period (T_{sw}) is calculated according to the following:

$$N = \lfloor V_{ref} \rceil$$
$$d = V_{ref} - \lfloor V_{ref} \rceil \tag{5.15}$$

Figure 5.9 illustrates the voltage waveform generation of an arm in a MMC with five submodules per arm using NLM.

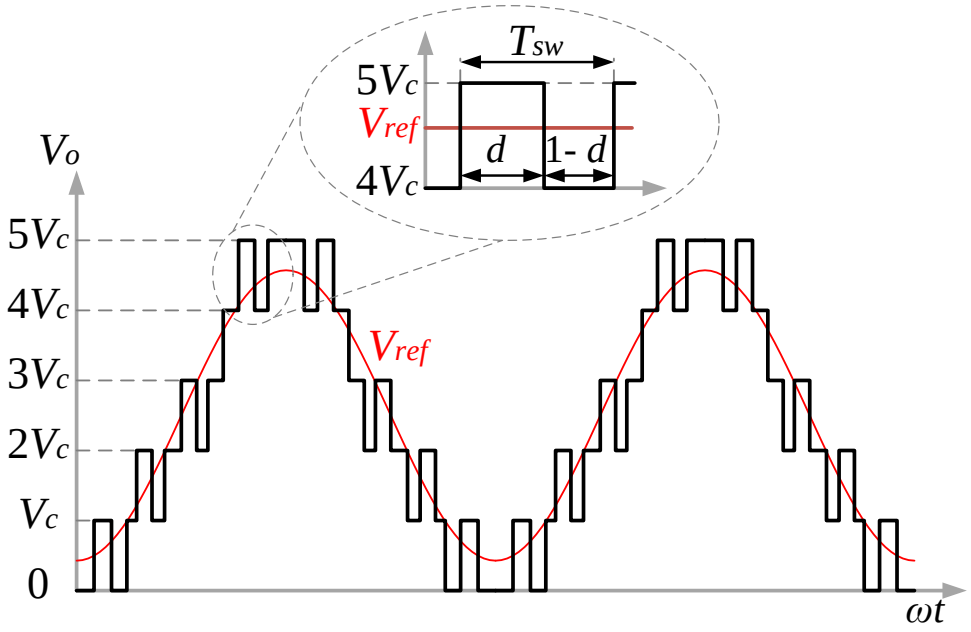


Figure 5.9. Voltage waveform generation of an arm in a MMC that has ten submodules per phase using NLM.

5.2.4. Selective harmonic elimination for MMCs

As in the case of NPC and CHB converters, the SHE for MMC is based on the off-line calculation of the switching angles for the converter devices according to mathematical equations derived from the Fourier series.

The basis of SHE for modular converters were explained in section 4.2.3 for a generic number of levels. Now the particular case of solving the SHE problem to modulate a 6-level converter eliminating the first fifteen odd non-triple harmonics will be explained.

The general expression for the amplitude of any harmonic in a multilevel waveform appeared in equation (4.9), and the general formulation for the SHE problem with a set of *N* angles was expressed in equation (4.10). According to those expressions, the formulation of SHE problem for a 6-level converter only needs a little change due to in a waveform with six levels there is not zero level (see Figure 5.10). So, in the case that concerns to us, the generic expression of any harmonic amplitude is:

$$h_n = \frac{4V_c}{n\pi}\left[\frac{1}{2} + \cos(n\theta_1) - \cos(n\theta_2) + \cdots + \cos\left(n\theta_{k_1}\right) + \cos\left(n\theta_{k_1+1}\right) - \cos\left(n\theta_{k_1+2}\right) + \cdots + (-1)^{N+1} \cdot \cos(n\theta_N)\right] \tag{5.16}$$

Equation (5.16) must to be understood having into account that the quarter-wave symmetry is used to generate the voltage waveforms, as in the previous explained cases.

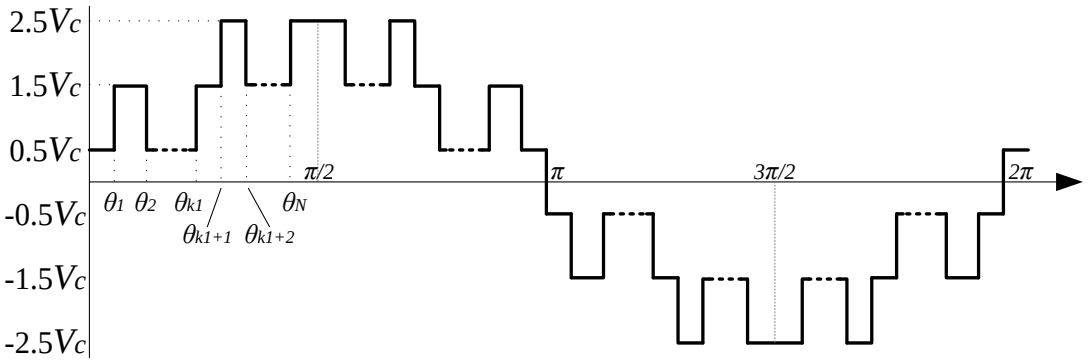


Figure 5.10. SHE waveform shape with N switching angles for a 6-level converter.

According to equation (5.16), the equations system to be solved in this case to eliminate fifteen harmonics in a 6-levels MMC (being $k_1 = 7$) is the following:

$$\begin{aligned}
f_1(\theta) &= \frac{1}{2} + \cos(\theta_1) - \cos(\theta_2) + \cdots + \cos(\theta_7) + \cos(\theta_8) - \cos(\theta_9) + \cdots + \cos(\theta_{16}) \\
&= \frac{\pi V_c}{4} m \\
f_2(\theta) &= \frac{1}{2} + \cos(5\theta_1) - \cos(5\theta_2) + \cdots + \cos(5\theta_7) + \cos(5\theta_8) - \cos(5\theta_9) + \cdots \\
&\quad + \cos(5\theta_{16}) = 0 \\
f_3(\theta) &= \frac{1}{2} + \cos(7\theta_1) - \cos(7\theta_2) + \cdots + \cos(7\theta_7) + \cos(7\theta_8) - \cos(7\theta_8) + \cdots \\
&\quad + \cos(7\theta_{16}) = 0 \\
&\vdots \\
f_{16}(\theta) &= \cos(47\theta_1) - \cos(47\theta_2) + \cdots + \cos(47\theta_7) + \cos(47\theta_8) - \cos(47\theta_9) + \cdots \\
&\quad + \cos(47\theta_{16}) = 0
\end{aligned} \tag{5.17}$$

As was explained in previous chapters, these equations are non-linear and transcendental, so an approximation method is needed to obtain the solution. In this case the genetic algorithms technique has been applied to solve the SHE problem with the explained characteristics. The solution can be found in Figure 5.11, and in Figure 5.12 is depicted the harmonic content of phase-to-neutral and phase-to-phase voltages when that solution is applied to a 6-level MMC.

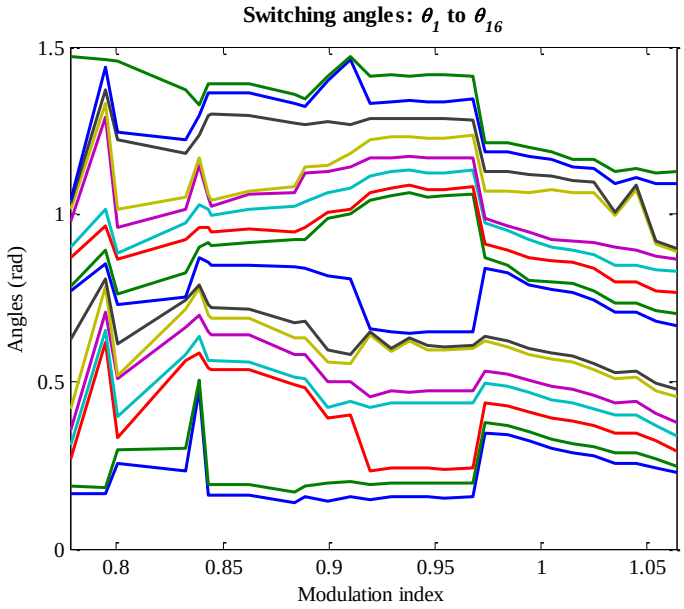


Figure 5.11. Solution set of angles for eliminating the first fifteen odd non-triple harmonics in a 6-level converter.

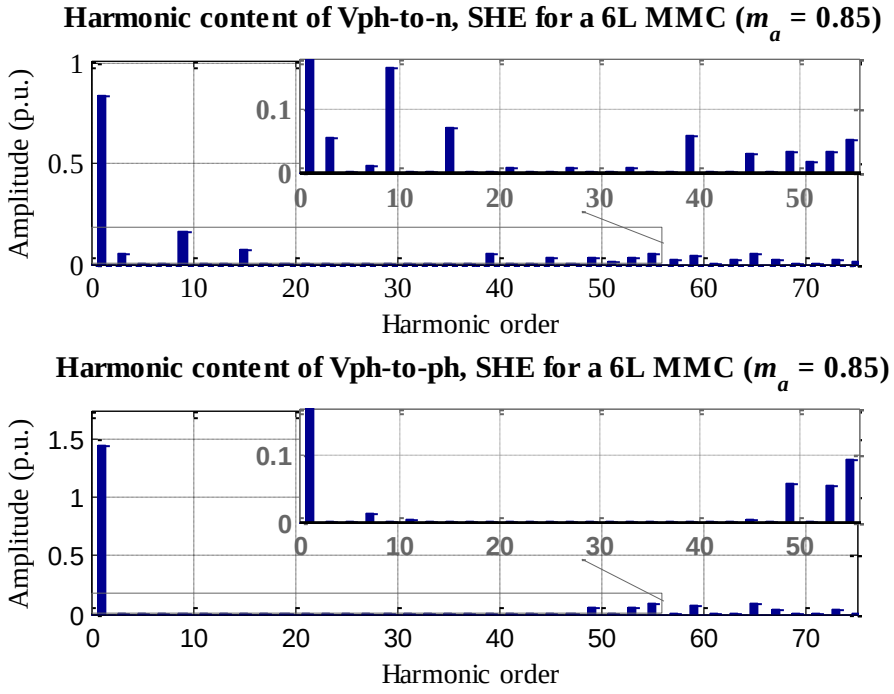


Figure 5.12. Harmonic content of the phase to neutral (up) and the phase to phase (down) voltages when SHE modulation is applied to a 6-level MMC to eliminate fifteen harmonics (ma = 0.85).

5.2.5. Capacitors voltage balancing algorithm

In this work, in order to balance the voltage between all the submodule capacitors in a phase, the method proposed in [109] is used. This algorithm acts over the switching signals, so

it is independent from the modulation method used. The moment of application of this voltage correction can be better understand seeing Figure 5.13.

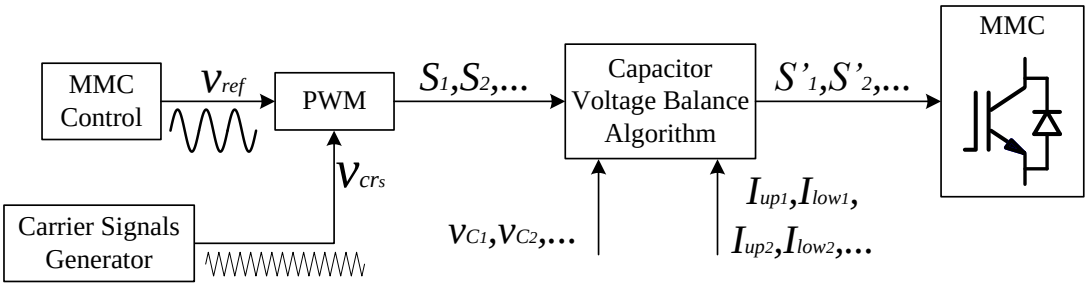


Figure 5.13. Block diagram of the application of the capacitors voltage balance method.

This algorithm works only if a capacitor voltage is over or under a certain threshold values. So if an imbalance is detected, the algorithm evaluates the current flow in order to identify if it is charging or discharging the capacitors: if the current flow is negative means that it is charging the capacitors; and if it is positive, it is discharging them. The next step is selecting which submodules switch on and which switch off. This task is done attending to the following criteria:

- If the current flow is negative the capacitors are charging, therefore the capacitor with the maximum voltage must be switch off and the capacitor with the minimum voltage must be switch on.

- Otherwise, if the current flow is positive the action should be opposite to the previous case: as the capacitors are discharging, the submodule with the minimum voltage is switch off in order to stop the discharge, and the capacitor with the maximum voltage is switch on with the aim to balance the voltages.

Figure 5.14 shows a flux diagram of this method operation.

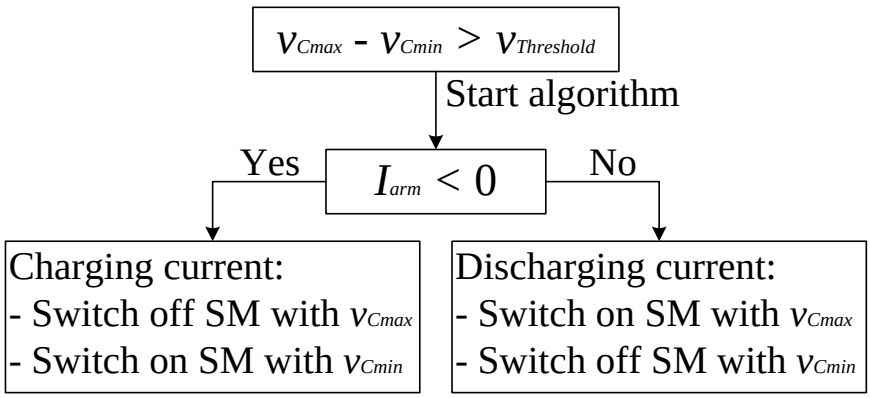


Figure 5.14. Flux diagram of the capacitors voltage balancing method.

5.3. MMC operation under fault condition

As in the case of CHB converter, there are some kinds of faults than can occur in a MMC converter. The worst one is a DC fault, and to protect the converter against this kind of fault, a thyristor is usually installed in parallel with each submodule in order to bring an alternative path for the current without causing damage in it, as it can be seen in the scheme of Figure 5.15.

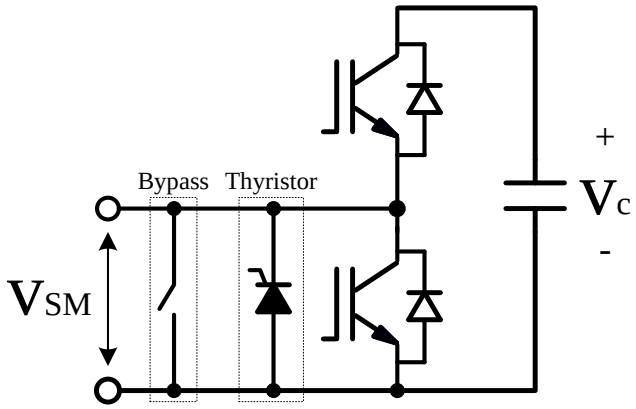


Figure 5.15. Scheme of a MMC submodule including the protection against DC fault.

Leaving apart other kind of faults, in this work is studied the case of fault in a submodule. In such case, the first thing to do is to bypass the damaged submodule in order to create an alternative path for the current. The opposite submodule in the complementary branch must be bypassed too in order to maintain even the number of submodules in the phase. According to that, the DC voltage is shared between the remaining submodules of the same phase, supposing this fact an increment in the capacitor voltage, Δv_C. This voltage increment can be calculated as

$$\Delta v(\%) = 100 \cdot \left(\frac{n}{n'} - 1\right) \tag{5.18}$$

where n is the original number of submodules in each phase, and n' is the number of remaining submodules after bypass the faulty one and its opposite.

Following equation (5.18), Figure 5.16 shows as the increment grows exponentially with the number of faulty submodules. In this scenario it is necessary to define where should be fixed the limit of the voltage increase in order to not damage the capacitors. Usually, the converters are designed with the guarantee to keeping working with a percentage of faulty submodules between 20% and 30%, what suppose an increment of the voltage between 25-45%. In this case, this author fixes as maximum having 50% of faulty submodules, what will be translated in double the voltage for the remaining submodules.

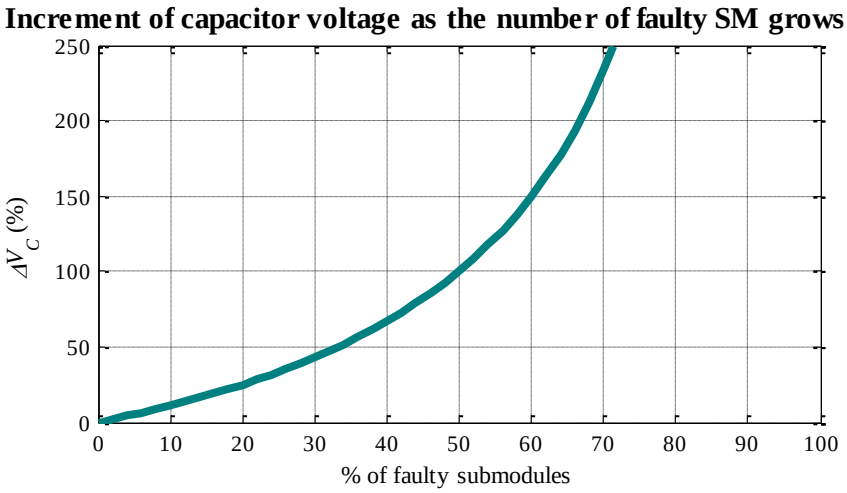


Figure 5.16. Illustration of how the increment in the capacitor voltage grows as the number of faulty submodules in a phase increases.

Having the previous into account, Figure 5.17 illustrates the process of actuation if a fault in a submodule is detected. In such case, as some submodules are bypassed the corresponding phase will have in its output a voltage signal with the same amplitude but with less levels, which mean worse THD. As in MMC the DC voltage is maintained during a fault, the fault-tolerant method explained in subsection 4.3.4 cannot be implemented.

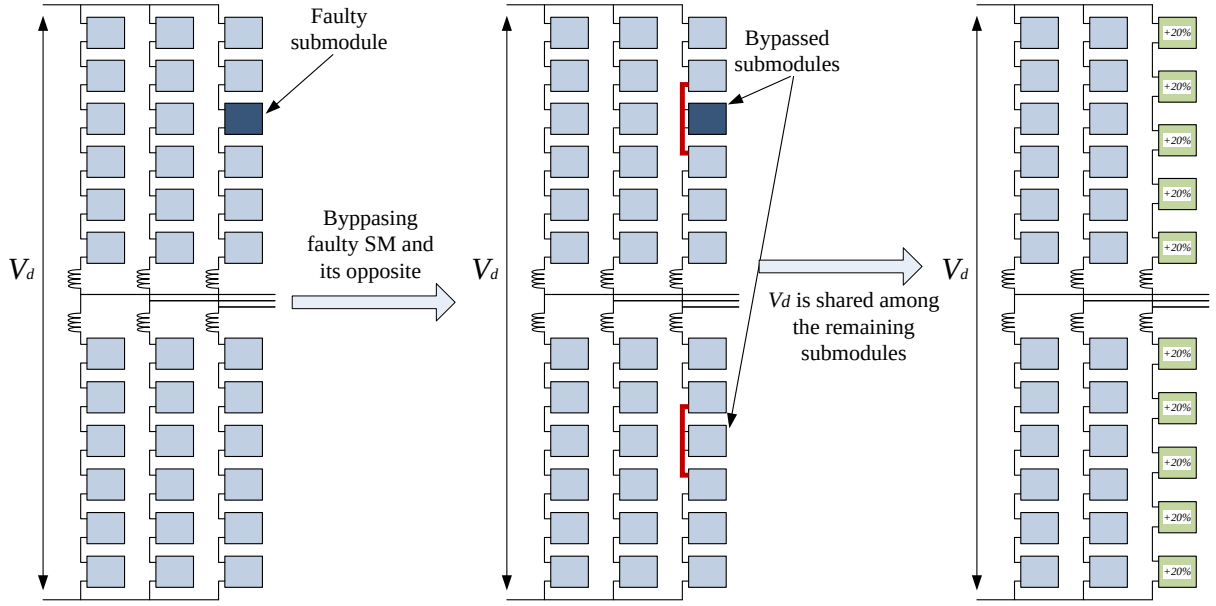


Figure 5.17. Illustration of the operation process in case of fault in a submodule.

Instead of that, one thing than can be done is rearrange the carrier signals in the phase with bypassed submodules in order to maintain the even symmetry in the output signal. This is done through the calculation of the angle between the carriers having into account the actual number of submodules:

$$\delta = \frac{2\pi}{\frac{n'}{2}} \tag{5.19}$$

According to the previous, in Figure 5.18 is shown an example of this technique and is illustrated how the harmonic content of the voltage signal corresponding to the phase with bypassed submodules improves, as the resultant voltage signal has even symmetry. In that figure, it can also be seen that bypassing the fault submodule and its opposite the number of levels of the output voltage changes from six to five. That is the reason why the harmonic content in the last case (with the bypassed submodules and the carrier signals rearranged) has its main band of harmonics closer to the origin than in the first case (without faulty submodules).

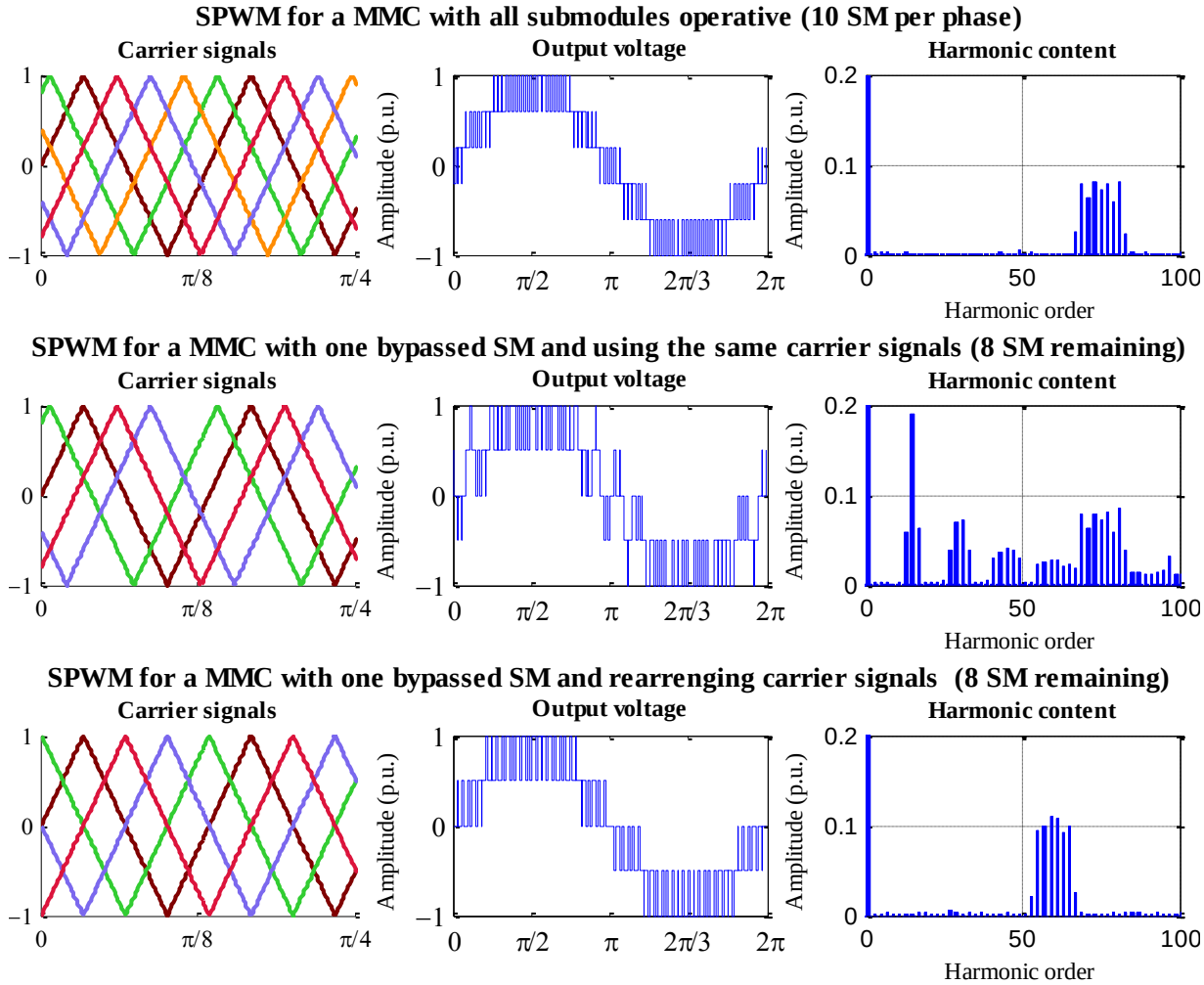


Figure 5.18. Illustration of the rearrangement done in the carrier signals when two submodules are bypassed in a 10-submodules (6-levels) MMC converter.

5.4. Applications for MMC converters

The modular multilevel converter was proposed as a solution for high voltage applications [110]-[112], especially for high voltage DC (HVDC) connections [113]-[117] and for wind power integration [118]-[120]. Over the years this topology has been developed also for other kind of applications such as battery energy store systems (BESS) [121], static compensators [122]-[124], and AC motor drives [125]-[128]. These two last cases have been studied in this work.

5.4.1. Power quality applications

As was said previously, MMC also has been used for grid connected applications. In this work the case of MMC used for a STATCOM system is studied in depth in Chapter 7, but the general scheme for this kind of connection can be seen in Figure 5.19.

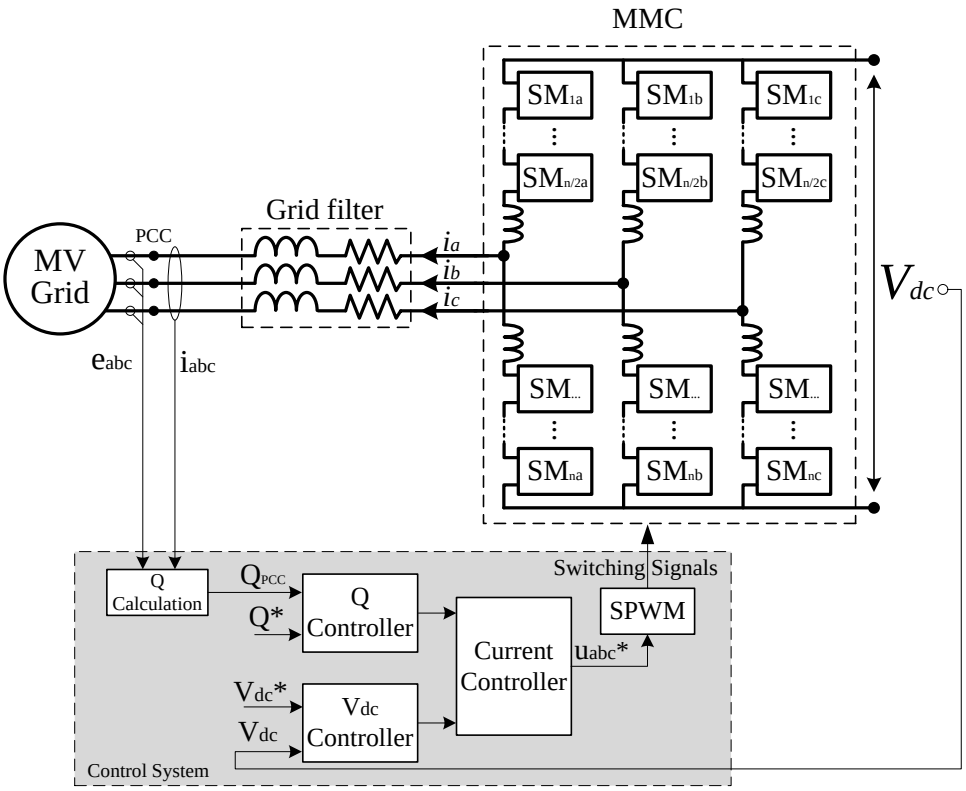


Figure 5.19. General scheme of a STATCOM system based on a MMC converter.

5.4.2. Drive applications

As in the previous case, the use of a MMC converter for an induction motor drive is studied in detail later. The basis scheme for this application appears in Figure 5.20.

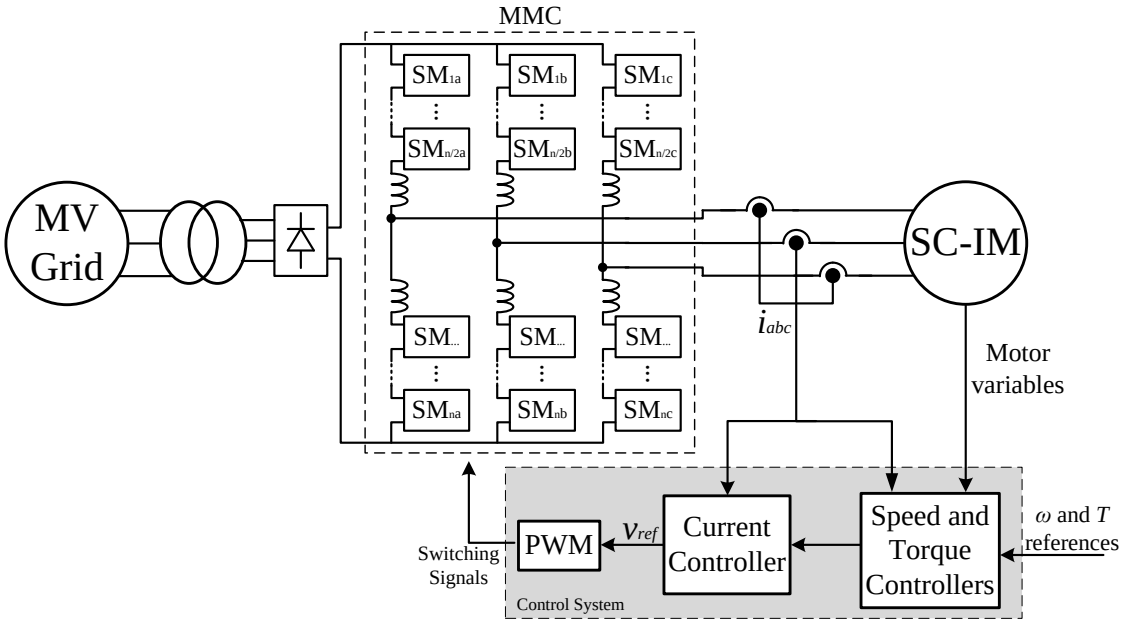


Figure 5.20. Basic scheme of motor drive using a MMC converter.

5.4.3. Peculiarities of MMC converter control

It is worth to mention that, whatever be the application in which the modular multilevel converter is used, it is necessary to implement some special controllers proper for this topology. On one hand, as was mentioned previously, due to the proper structure of this converter circulation currents are generated. These circulating currents get worse the harmonic content of the output signals, so it is advisable to implement controllers to try to eliminate them.

On the other hand, it is important that the voltage in all submodules is as better balanced as possible to guarantee a right operation. For this purpose it is advisable to implement a capacitors voltage balancing method like the explained in subsection 5.2.5.

Chapter 6: EXPERIMENTAL SETUPS

This Thesis work has been developed in the University of Alcalá, within the Group of Electronic Engineering Applied to Renewable Energy Systems (GEISER for the Spanish acronym). This research group has in its laboratory some prototypes that have been used in this work and in which the author has collaborated in different stages of their development. Also some tests have been done in a medium-voltage CHB prototype built by the company *Sedecal Control*, which is a partner of the GEISER group. The author of this thesis has collaborated in the development of some control algorithms for that prototype.

Before presenting different experimental results, those prototypes are described in this chapter. Specifically the prototypes that have been used and that are described in this chapter are the following:

- a back-to-back DNPC converter that was built in 2005, and in which this author has tested some control algorithms.

- a nine-levels cascaded H-bridge converter fully designed and built by this author under the supervision of her mentor.

- a thirteen-levels cascaded H-bridge converter designed and built by the company *Sedecal Control* with the collaboration of the GEISER group, and

- a six-levels modular multilevel converter fully designed in the GEISER group, and in whose start up this author has collaborated.

6.1. Back-to-back diode neutral point-clamped converter

The DNPC prototype existing in the GEISER research lab was developed in collaboration with the company *Sedecal Control* as a part of the project CONDOR II (ENE2005 08721 C04-01). The final result of this project is a 100 kVA back-to-back DNPC converter controlled through a control board based on DSP and FPGA.

This prototype can be divided in two well-differentiated parts: the power system and the control board. These parts will be described in the following subsections, and their relationships can be seen in Figure 6.1.

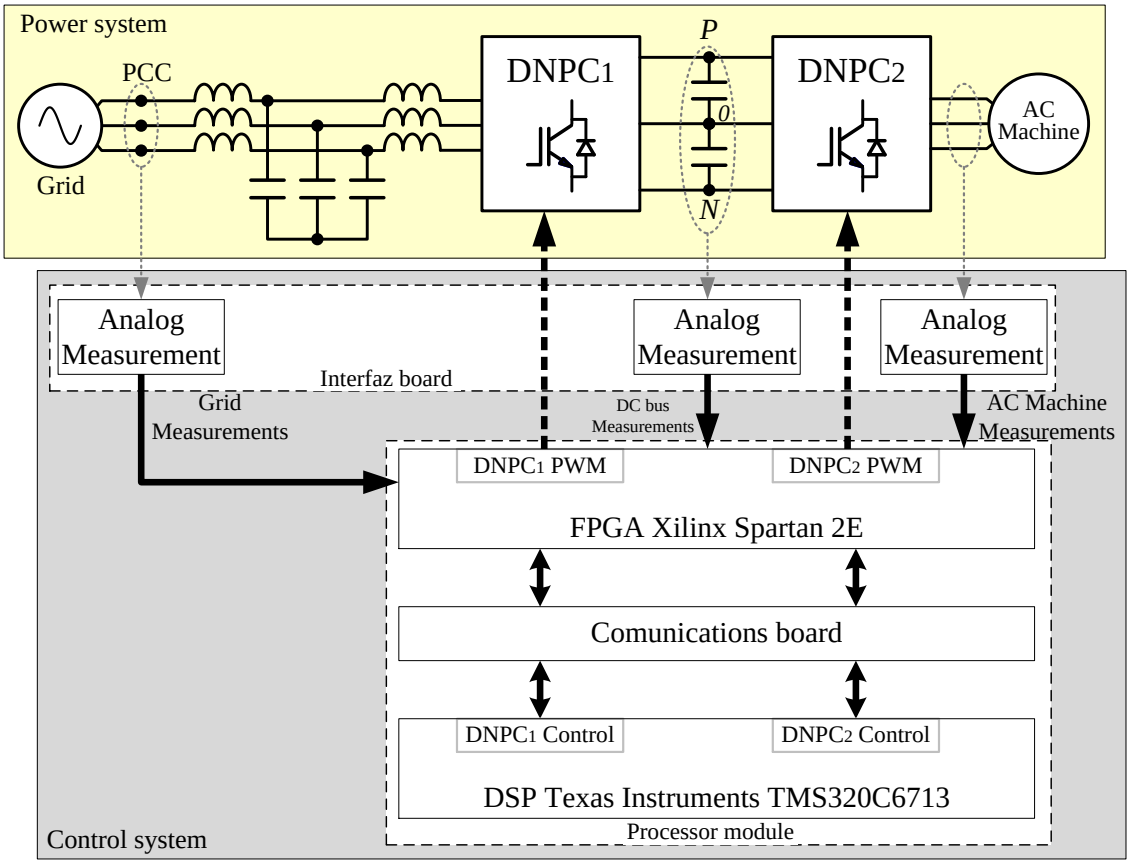


Figure 6.1. Diagram of back-to-back DNPC prototype.

6.1.1. Power system description

The power system is shown in Figure 6.2, and it is composed by the two DNPC converters and the grid filter that in this case is type LCL. The first DNPC converter is connected to the grid through the LCL filter, and the second converter is connected to an AC machine. This structure is bidirectional, what means that it can be used to operate the AC machine with power from the grid, and also it could be used as an energy generator.

The main characteristics of the power system are summarized in Table 6.1.

Table 6.1. Main characteristics of the DNPC prototype power system.

Nominal Power		100 kVA
Nominal Voltage		400 V_{AC}
Maximum DC voltage		1200 V
DC capacitors		2000 μF / 750 V_{DC}
IGBTs		FD300R12KE3 DF300R12KE3
Filter	**L_1**	0.5 mH / 175 A_{rms}
	L_2	0.25 mH / 150 A_{rms}
	C_o	100 μF / 400 V_{AC}

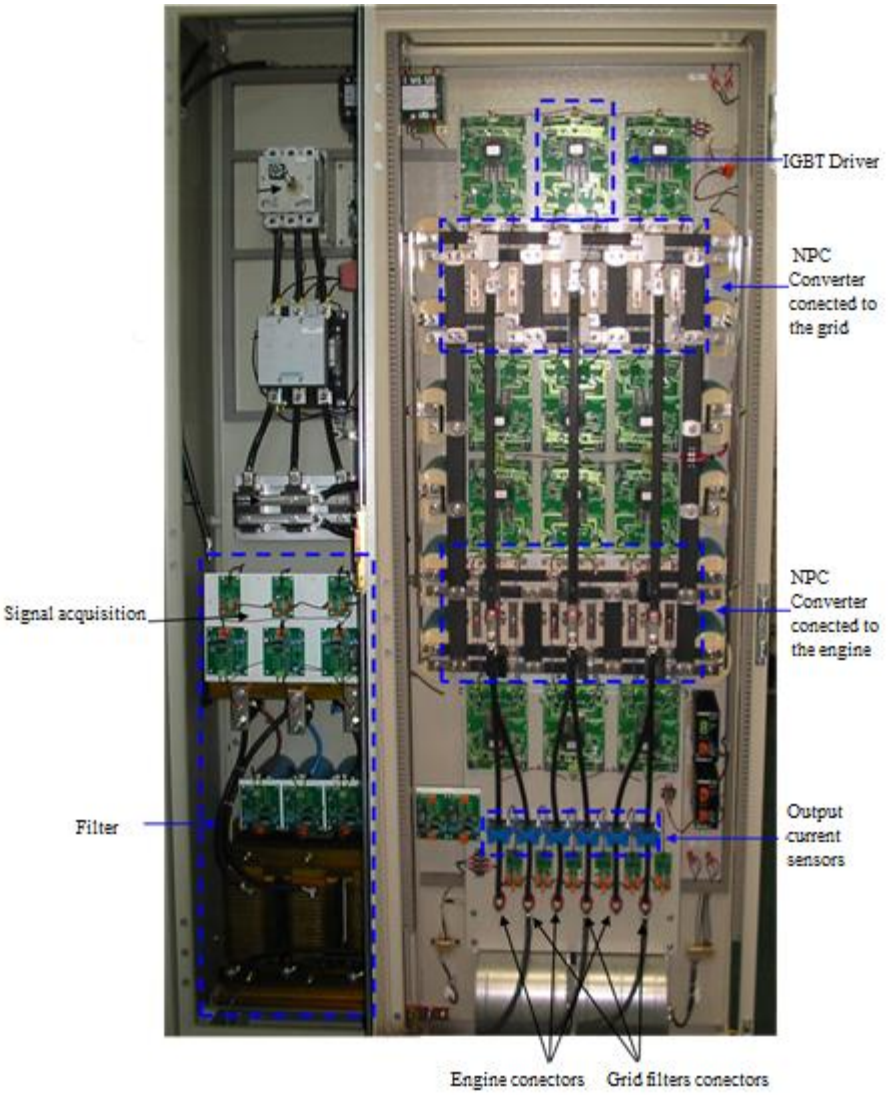


Figure 6.2. Two DNPC converters in back-to-back configuration that are in the GEISER research laboratory.

6.1.2. Control system description

The prototype control system consists on a DSP and a FPGA working together in the same processing board. This system was designed to meet the following requirements:

- Being flexible enough for its use in research projects and in final prototypes, and allowing an easy programming in C language, and the direct compilation from Matlab/Simulink.

- Having computational capacity enough to implement complex algorithms into it.

- Being a scalable platform and allowing its connection to other control systems that could operate at the same time in the case to be used in a distributed system.

To meet those objectives, the control platform is split into two subunits: the first one, containing the DSP, has as main target the efficient resolution of high grade computational algorithms; the second one that includes the FPGA and other electronic elements is responsible of implementing the configurable logic to perform the communications, the data acquisition, and other auxiliary functions.

Figure 6.3 shows the designed multiprocessor board, and the tasks distribution between both processors is summarized in Table 6.2

Figure 6.3. Control board for the DNPC converters, which is based in DSP+FPGA.

Table 6.2. Tasks distribution between DSP and FPGA.

DSP
Current controllers
Reference frames transformations (*abc* ↔ *dq*)
DC-bus voltage controller
Grid monitoring
FPGA
Global synchronization of multiprocessor system
PWM generation
Processing input/output signals

6.2. Cascaded H-bridge converter built in GEISER research lab

The CHB converter that is in the GEISER research lab is a nine-levels (four-cells), 50 kVA prototype. The prototype design was done allowing the use of CHB converter in power quality applications and also as a drive system, with only doing changes in the control code. Moreover, it was designed with the possibility to bypass three of its twelve cells in order to test fault-tolerant methods.

The CHB prototype is composed of 12 cells distributed in three phases, a multi-pulse transformer that supplies the 12 independent DC voltages to feed the cells, and the hardware control platform that is based in dSPACE and in a Microzed System-on-Chip board.

Figure 6.4 shows a general scheme of the CHB prototype. As the reader can see, operating adequately circuit breakers 1, 2, and 3, the system can be configured as a drive or as a power quality application. In Figure 6.4 also are represented with a different color the three cells that can be bypassed (B1, C1, and C2). In the next subsections the subsystems in which is divided the prototype are explained: the power system and the control system.

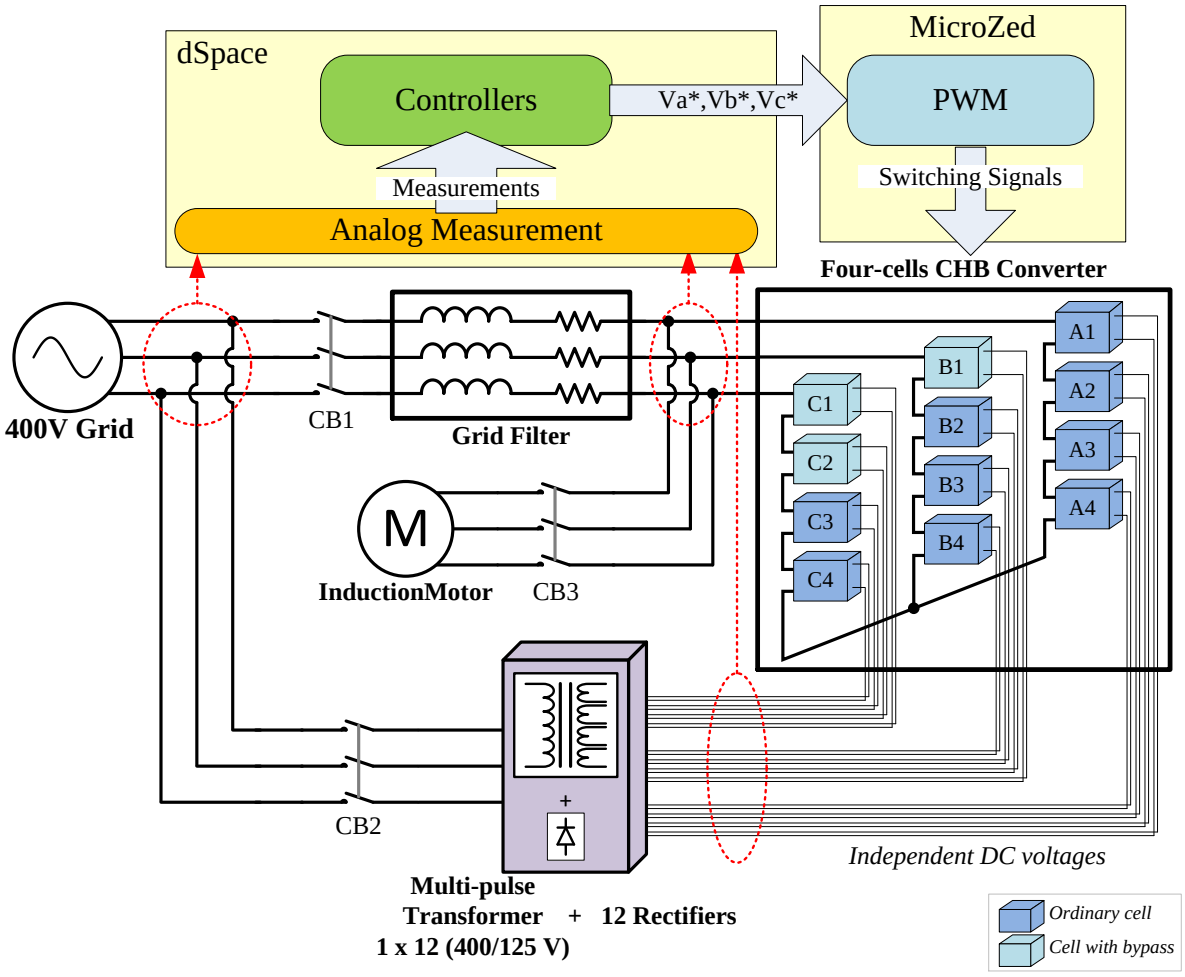


Figure 6.4. General scheme of the CHB prototype existing in GEISER research laboratory.

6.2.1. Power system of CHB prototype

The CHB prototype that has been built in the laboratory is represented in the scheme shown in Figure 6.5. The converter is composed by four cells per each branch that are feed by a multi-pulse transformer. Each of the cells is based in two half-bridge devices and a capacitor of 3900 μF. In Figure 6.6.a) the real prototype appears: cells A1, A2, B1, B2, C1 and C2 are sited in in the right locker, and the rest of the cells are located in the left one. The features of the components that compose the cells of the converter are summarized in Table 6.3.

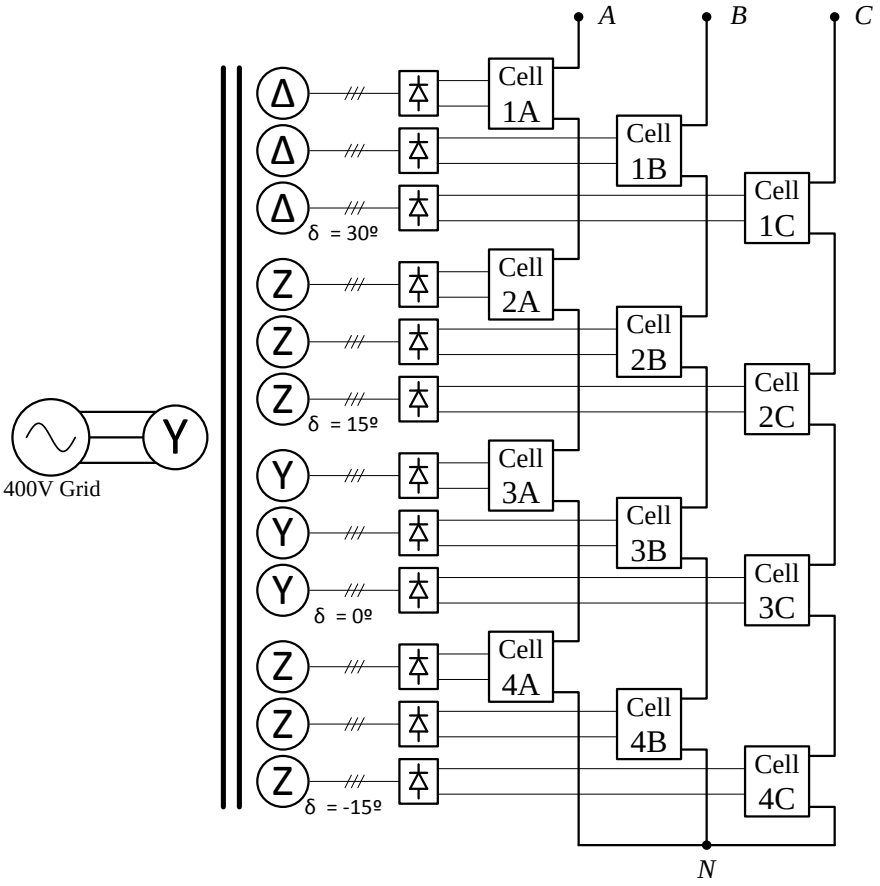


Figure 6.5. Scheme of the CHB converter and multi-pulse transformer.

Table 6.3. H-bridge cells main features.

Half-bridges (two per cell)	Fuji '2MBI300U4N-170-50'
Drivers (one per half-bridge)	SCALE-2 Plug&Play Driver '2SP0115T2A0-12'
Capacitors (one per cell)	Nichicon 'LNY2G392MSEH' (3900 μF, 400 V)

In order to minimize the harmonic currents in the system the multi-pulse transformer (Figure 6.6.b)) must be designed correctly with appropriated phase displacements between its windings. In this case, as four cells per phase must be fed, the displacement is 15º between windings (for better understanding the design process, see Appendix A). Table 6.4 summarizes the main characteristics of the multi-pulse transformer that has been built for this prototype.

Connected to each output winding is a rectifier ‘Semikron SKD 83-16’ that supplies the DC voltage for each cell.

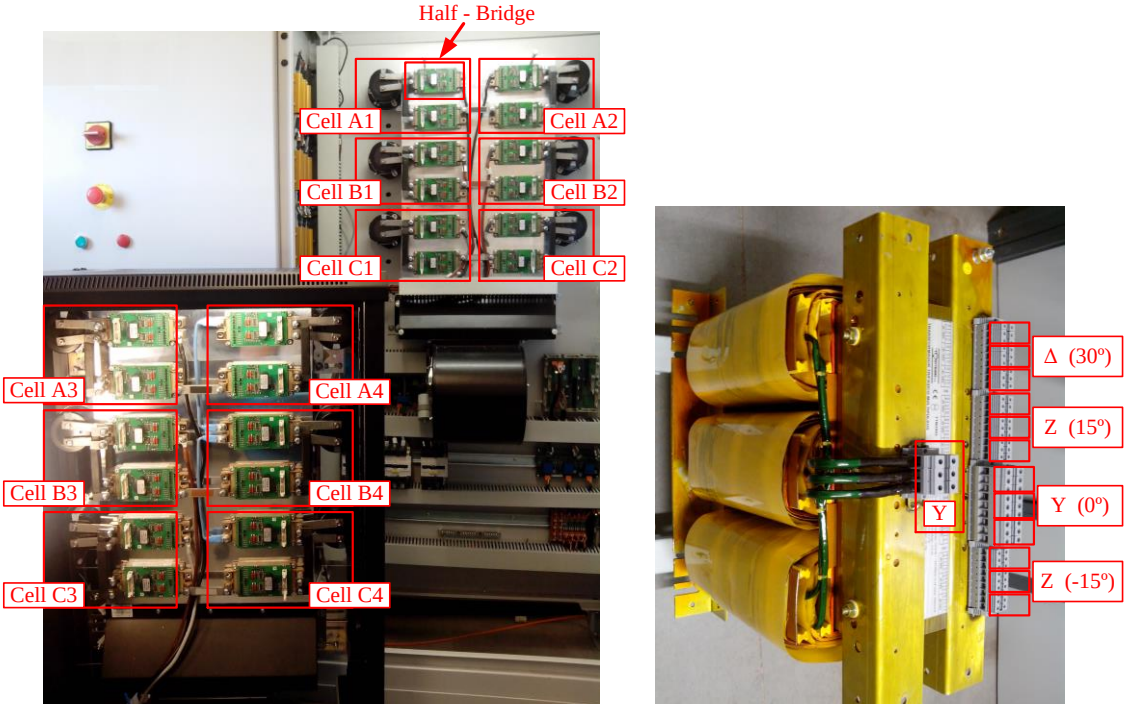


Figure 6.6. Illustration of the 12 cells that compose the CHB converter a); and the multi-pulse transformer used to feed them b).

Table 6.4. Characteristics of multi-pulse transformer used to feed CHB converter.

Nominal Power	50 kVA
Primary Voltage	400 V
Secondary Voltage (each winding)	125 V
Phase displacement – Connection	
Primary winding	Star
Secondary winding 1	30º – Delta
Secondary winding 2	15º – Z-1
Secondary winding 3	0º – Star
Secondary winding 4	-15º – Z-2

6.2.2. Control system for the CHB prototype

In order to control the proposed prototype a hardware platform has been designed and implemented, which is composed of a dSPACE platform and a Microzed System-on-Chip board.

The advantage of use a fast prototyping platform like dSPACE is that the control algorithms can be implemented directly in Simulink format, as this tool allows linking its own software with Matlab/Simulink. The main drawback in this case was that as there are twelve cells in the converter, 48 switching signals are need, and this quantity was not available for the dSPACE system existing in the lab. So, the adopted solution was implementing the control algorithms and generating the reference voltage signals for the three phases with dSPACE, and sending these signals to the Microzed SoC board where the switching signals are calculated.

So, on one hand, the commercial dSPACE platform is the responsible to execute the control algorithms and to acquire the required analogic signals, and on the other, the SoC board is used to generate the Pulse-Width Modulation (PWM) signals. The control system designed is represented in Figure 6.7, and it works as follows:

- The signals are measured by the sensors board, and the data acquisition is performed by the DS4003 A/D board.

- The DS1006 processing board executes the control algorithms and the reference voltages and circuit breakers control signals are obtained. The algorithms and controllers are programed directly in a Simulink model and then this model is compiled to be used in the dSPACE.

- The reference voltage is sent through the DS2004 digital I/O board to the Microzed, where the PWM is generated. Also through the DS2004 board the control signals for the circuit breakers are sending.

- The PWM signals are generated using the Programmable Logic (PL) part of this board. For this purpose carrier based PWM is used.

- Finally, the PWM signals are applied to the IGBTs.

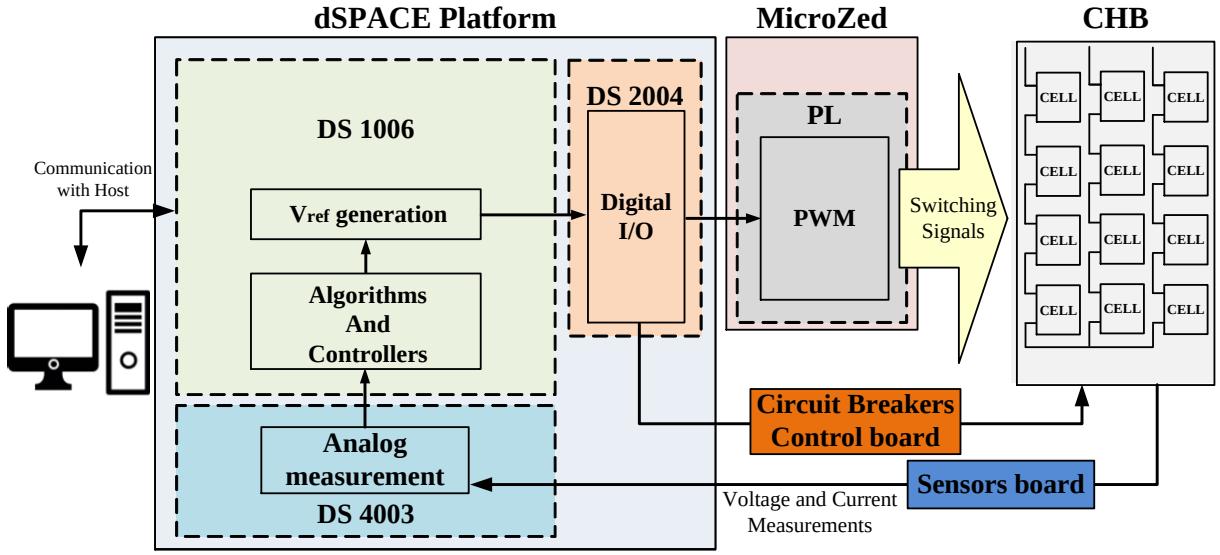


Figure 6.7. Representation of the control platform designed for the CHB converter.

Figure 6.8 shows the Microzed based SoC board for generating the PWM signals.

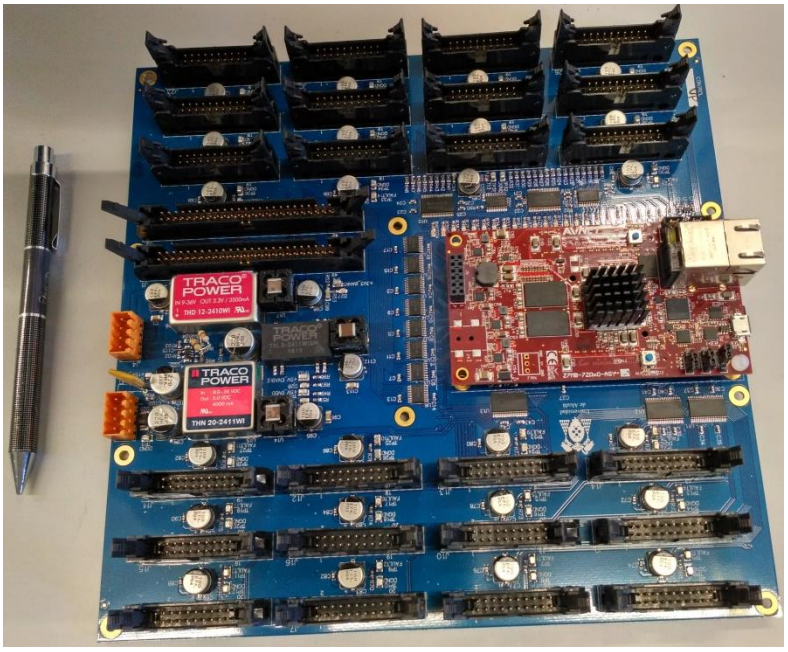


Figure 6.8. Illustration of SoC board based on Microzed.

6.3. Thirteen-levels CHB prototype built by *Sedecal Control*

As was mentioned at the beginning of this chapter, some of the tests included in this Thesis have been done in a six-cells thirteen-levels CHB prototype owned by *Sedecal Control*, which has been designed to work as a medium-voltage drive. The description of this prototype is included in this chapter because it has been developed as a collaboration project between this company and the GEISER group, and this author has collaborated in the development of some of the control algorithms for this converter. In the following subsections the power and control systems of this prototype will be explained. As there is a no-disclosure agreement (NDA) related to this prototype, only the non-protected information will be included in this section.

6.3.1. Power system of the thirteen-levels CHB prototype

As it was previously said, the prototype build by this company is a six-cells CHB designed to feed 6600 V induction motors. The main scheme of this prototype of medium-voltage drive is depicted in Figure 6.9. As it can be seen in that picture, the system is composed by a multi-pulse transformer and the eighteen cells cascaded connected that feeds the induction motor. The characteristics of the multi-pulse transformer are summarized in Table 6.5, and Figure 6.10 and Figure 6.11 illustrate the real prototype.

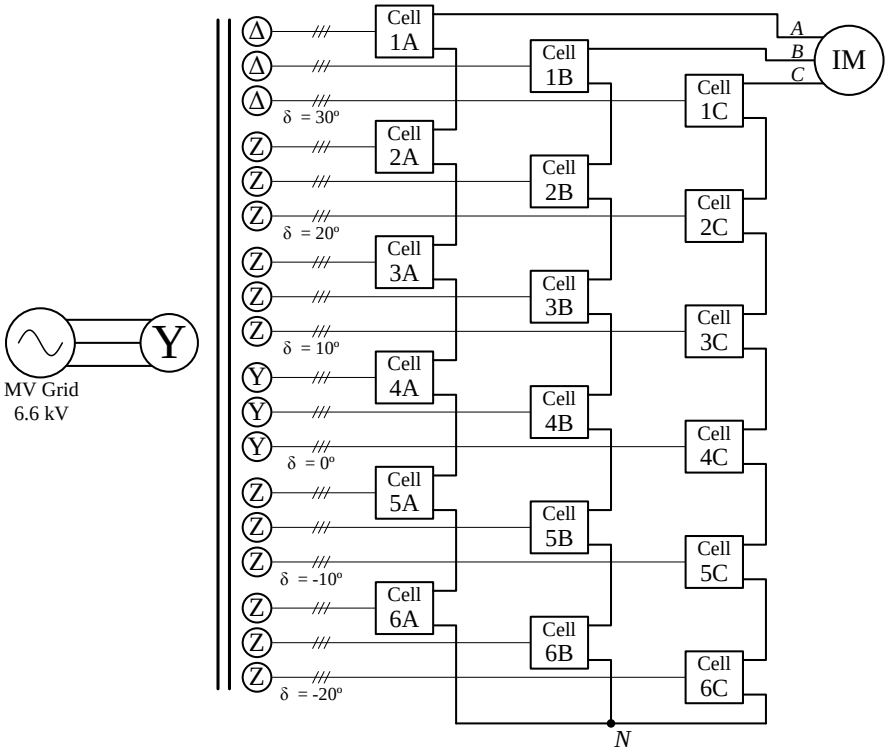


Figure 6.9. Main scheme of the six-cells thirteen-levels CHB prototype build by Sedecal Control.

Figure 6.10. Illustration of the six-cells CHB converter developed by Sedecal Control.

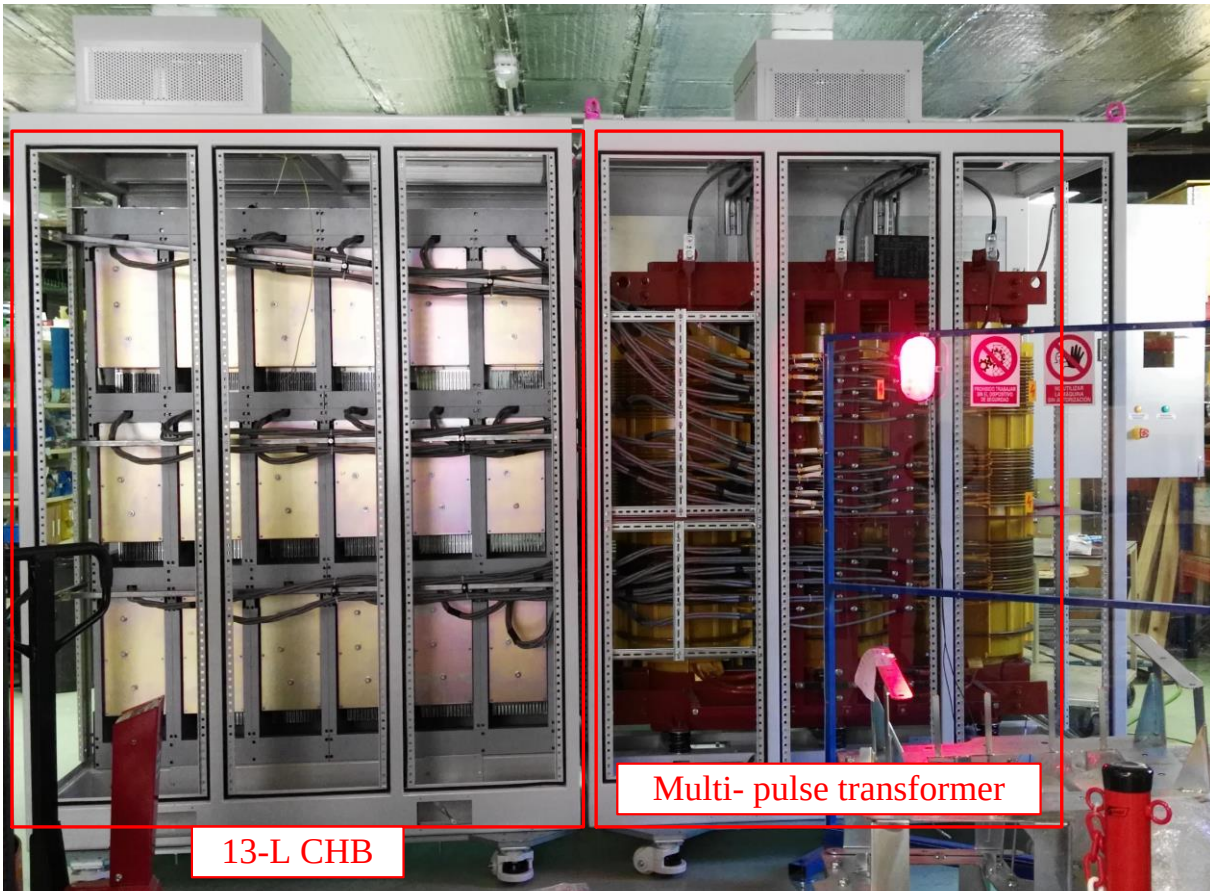


Figure 6.11. Back view of the thirteen-levels CHB prototype: the converter (left side) and multi-pulse transformer (right side).

Table 6.5. 18-secondary windings multi-pulse transformer parameters.

Nominal Power	1.5 MVA
Primary Voltage	6.6 kV
Secondary Voltage (each winding)	760 V
Phase displacement – Connection	
Primary winding	Star
Secondary winding 1	30º – Delta
Secondary winding 2	20º – Z-1
Secondary winding 3	10º – Z-1
Secondary winding 4	0º – Star
Secondary winding 5	-10º – Z-2
Secondary winding 6	-20º – Z-2

6.3.2. Control system of the thirteen-levels CHB prototype

For the control of the thirteen-levels CHB prototype the main requirement is the high number of signals to be acquired from and sent to the converter. In order to handle such

number of signals, in this case a hardware platform based on a Xilinx ZC702 System on Chip was chosen. To communicate that platform with the distributed boards that control each of the cells, there is an interface board. The main control system for this converter is very similar to that what will be widely explained in the following section for the MMC prototype. Figure 6.12 illustrates the two platforms that compose the main control system for this prototype: the ZC702 SoC platform (in the lower part), and the interface board (in the upper part). Once the control algorithms are executed in that platform, corresponding control signals are sent to the distributed control boards that control the modulation of each cell.

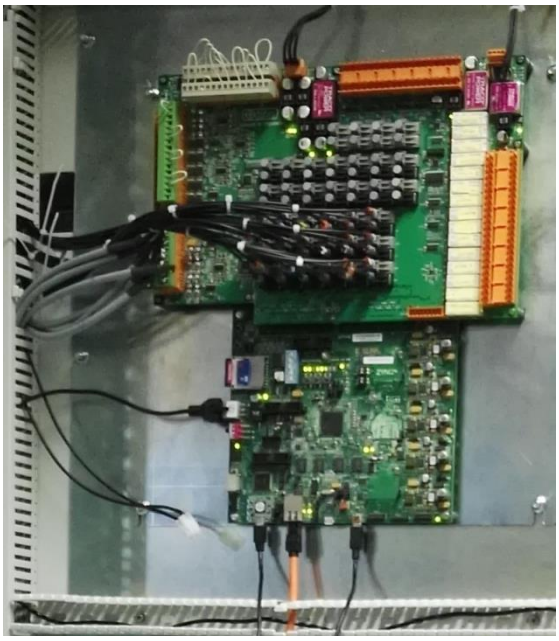


Figure 6.12. Illustration of the control system for the six-cells CHB prototype.

6.4. Modular multilevel converter

The MMC prototype existing in the GEISER research laboratory is a six-levels (ten submodules per phase) converter. As in the previous cases, the prototype is composed by the power system and the control platform used to implement the algorithms and controllers.

6.4.1. Power system of the MMC prototype

In this case, the prototype is a six-levels MMC converter. This converter is composed of ten submodules per phase (five in each arm), which have half-bridge configuration. So, in the converter there are a total of 30 half-bridge modules that in this case are IGBTs. Each submodule can handle up to 150 A, and 600 V, and the nominal power of the converter is 25 kVA. Table 6.6 summarizes the main characteristics of this converter.

The general illustration of the MMC prototype is in Figure 6.13. In the upper side the three phases are located, and in the bottom part are the circuit breakers to connect the converter to the grid, and also the control board. Figure 6.14 shows in detail one phase, where

it can be seen the ten drivers corresponding with the ten half-bridges (sited behind the drivers) that compose the phase, and the voltage sensors for each submodule.

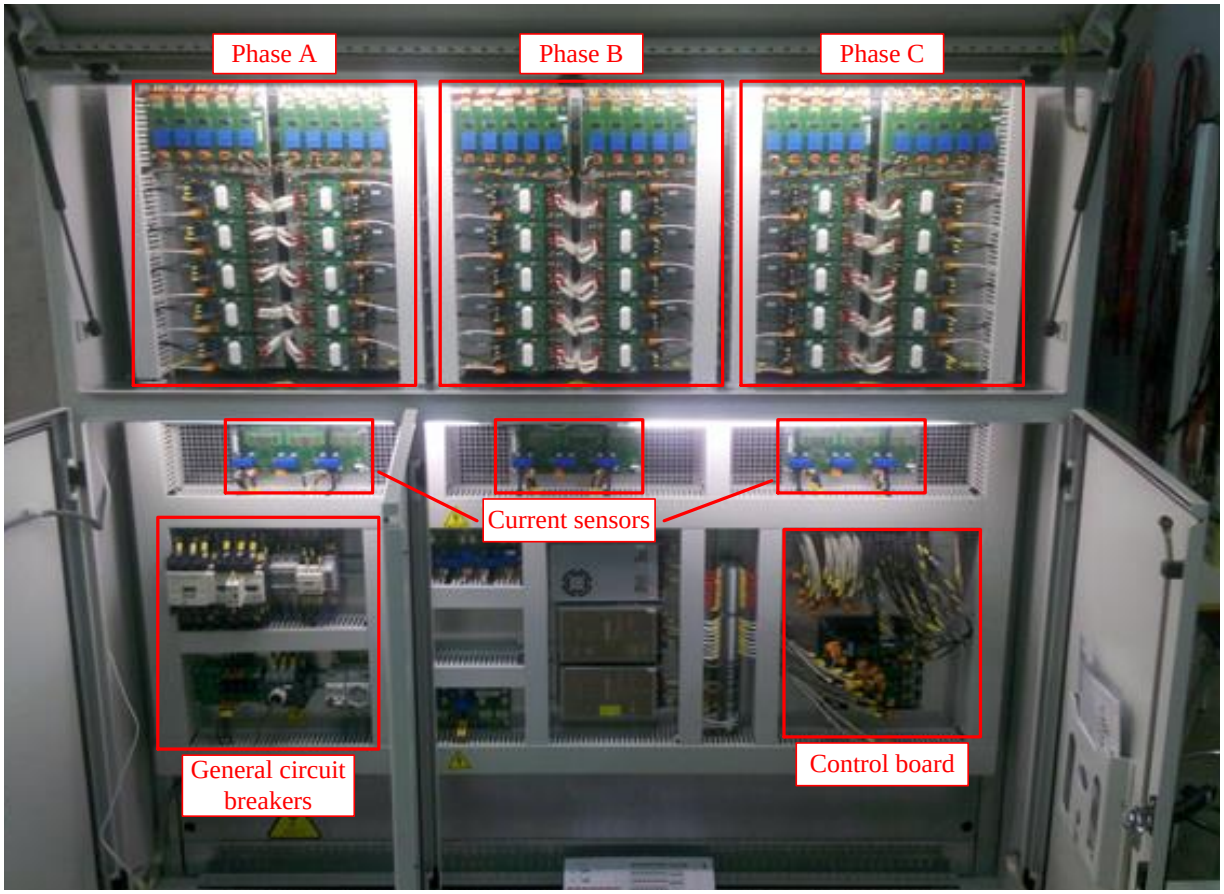


Figure 6.13. Illustration of MMC prototype.

Table 6.6. MMC prototype main parameters.

Nominal Power	25 kVA
Nominal Voltage	400 V
Half-bridge (one per submodule)	'SKM145GB066D'
Drivers (one per half-bridge)	'Skyper 32 R UL'
Capacitors (one per submodule)	2200 μF
DC-bus Voltage	1200 V
MMC inductor	0.5 mH
Grid inductor	5 mH

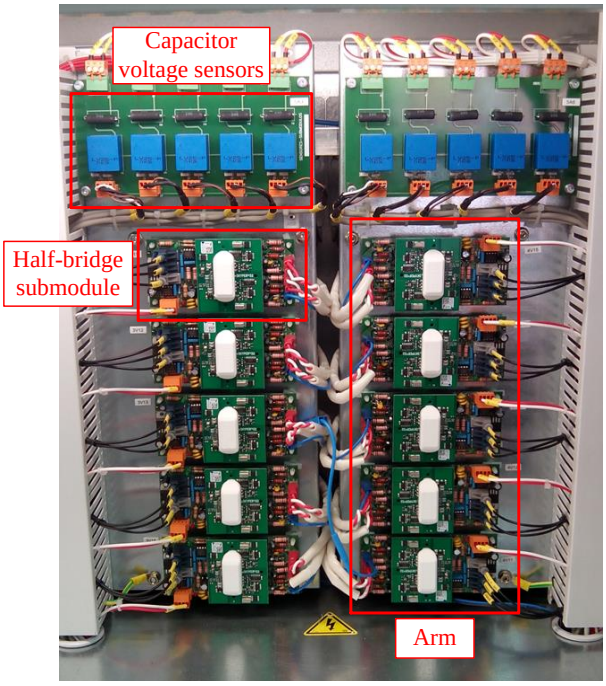


Figure 6.14. Detail of one phase of the MMC prototype.

6.4.2. Control platform for the MMC prototype

The huge amount of signals to be measured in the MMC require the hardware platform to have high performance in order to process all the signals properly. As any commercial platform with the desired features was found, the control platform was full in-house designed.

The designed hardware platform consists of two boards interconnected: the main of them is the ZC702 evaluation board manufactured by Xilinx, and it is based on a Z-7020 System-on-Chip; the second one is a custom interface board.

The ZC702 board has two main tasks, on one hand the communication with the computer, and on the other the execution of power converter control algorithms. Taking advantage of the two ARM cores presented in the board, these tasks are performed in different cores reducing the processing time.

The interface board acts as an interface between the power converter and the ZC702 board. Its function is adapting the signals that are exchanged with the converter. The board has the following features:

- 48 analog input signals
- 64 fiber optics transceivers
- 32 fiber optics receivers
- 4 Input relays
- 6 Output relays

The interface board is connected to the core board through the FPGA Mezzanine Card (FMC). Figure 6.15 shows both boards interconnected.

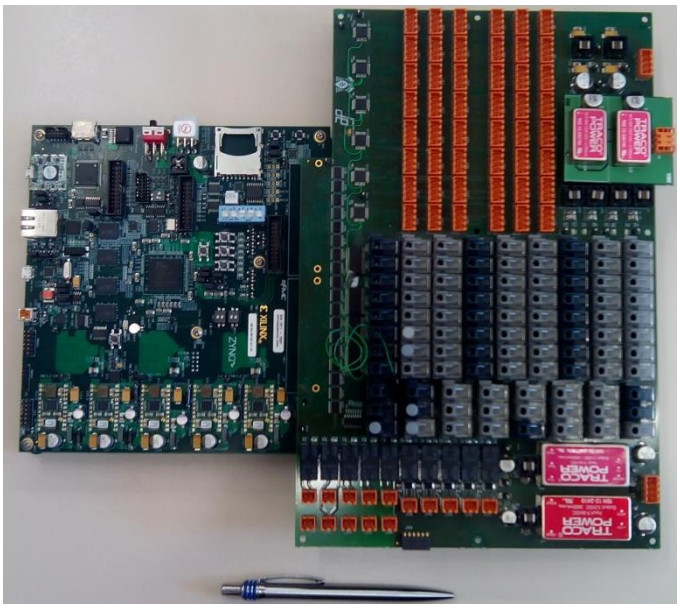


Figure 6.15. Designed hardware platform for the MMC prototype.

Chapter 7: TOPOLOGIES COMPARISON AND RESULTS

In this chapter a comparison between the studied topologies is done. First of all, a general comparison is done in order to show the advantages and drawbacks of each one, and after that some results obtained using these topologies in simulation models of different applications are summarized. GEISER research group has been working in the field of multilevel converters since 2002, and all the simulation models related to the controllers used in the developed work have been validated with experimental results previously. So that, the main aim of this chapter is to validate, by means of experimental results, the theoretical studies of modulation techniques and fault-tolerant methods of the multilevel topologies analyzed in this work.

Moreover, in this chapter some simulation and experimental results of the application of the fault-tolerant method for the CHB converter explained in subsection 4.3.4 are summarized. Also some experimental results obtained with the DNPC and MMC prototypes working in STATCOM systems are included in this chapter.

7.1. General comparison of the studied topologies

The studied topologies (DNPC, ANPC, CHB and MMC) can be compared attending to a lot of parameters. Table 7.1 shows their comparison based on the most representative of those parameters. For the modular topologies (CHB and MMC) some of the parameters are expressed as a function of their number of cells or modules per phase (n), and also for two examples: 3-levels case, and 9-levels case.

As it can be seen in Table 7.1, the main difference between the neutral point-clamped topologies and the other studied topologies is that these last ones are modular, and this fact allows increasing the number of levels in the phase-to-neutral output only adding modules in the phases of the converter. As drawback, the number of active devices increases as the number of modules grows, and hence the number of control signals also does, what means that the modulation method has to manage this increase. In terms of DC voltage supply, the difference is that the MMC and the neutral point-clamped topologies work with a single DC source; meanwhile the CHB converter needs an isolated DC-source for each cell.

The differences between topologies when they are implemented in some applications are summarized in the following section; specifically the topologies have been tested as STATCOM, and in an induction motor drive.

Table 7.1. General comparison between the studied topologies.

	NPC		***CHB***	***MMC***
	DNPC	***ANPC***		
Number of levels	3 (fixed)	3 (fixed)	$2n + 1$ (variable) Example 1: 3 lev.(n =1) Example 2: 9 lev.(n =4)	$n/2 + 1$ (variable) Example 1: 3 lev.(n =4) Example 2: 9 lev.(n =16)
Modularity	No	No	Yes	Yes
DC-side connection	Connected (V_d)	Connected (V_d)	Isolated ($3n$ x E)	Connected (V_d)
Max/Min Output voltage (Ph-to-N)	$\pm V_d/2$	$\pm V_d/2$	$\pm nE$ (Ex1: $\pm E$) (Ex2: $\pm 4E$)	$\pm n/4\ V_C$ $V_C = 2V_d/n$ (Ex1 & Ex2: $\pm V_d/2$)
Fault-tolerant	No	No	Yes	Yes
Number of active devices (3-phases case)	12	18	$3 \cdot 4 \cdot n$ (Ex1: 12) (Ex2: 48)	$3 \cdot 2 \cdot n$ (Ex1: 24) (Ex2: 96)
Number of non-active devices (3-phases case)	6	0	0	0
Number of capacitors (3-phases case)	2	2	$3 \cdot n$ (Ex1: 3) (Ex2: 12)	$3 \cdot n$ (Ex1: 12) (Ex2: 48)
Bidirectional behavior	Yes	Yes	No	Yes

7.2. Comparison of topologies implementation in different applications

The explained topologies have been simulated in Matlab/Simulink as part of a STATCOM, and of an induction motor drive. All the theoretical studies have been done in medium voltage models, but as, following safety standards, GEISER research lab has not

available a MV connection, also low voltage models have been developed, and these last ones have been used to obtain the results shown in this section.

All the controllers used in those simulations have been designed to be adaptable from MV to LV, and vice versa. For each one of the selected applications, the models for the four topologies have been designed in such way that the controllers have the same parameters regardless of the used topology.

The parameters compared after testing the simulation model with the different applications are the controller's response for each topology, the harmonic content of the converters output signals, and the devices losses for the different topologies.

7.2.1. STATCOM simulation models

These simulations have been done in order to compare between them a 3L-ANPC, a 3L-DNPC, a 9L-CHB (4-cells per phase), and a 9L-MMC (16-submodules per phase).

The description and operation for a STATCOM system is described in detail in Appendix B. Figure 7.1 shows the general scheme used in this case, where a reactive power controller and a DC voltage controller have been implemented. The first of them controls that the reactive power generated or consumed by system follows its reference, and the second one is responsible of maintain the desired DC voltage for the converter. These controllers outputs are the references i_d* and i_q* for the current controllers, whose outputs are the *dq* voltage references used to generate the switching signals for the chosen voltage source converter in each case.

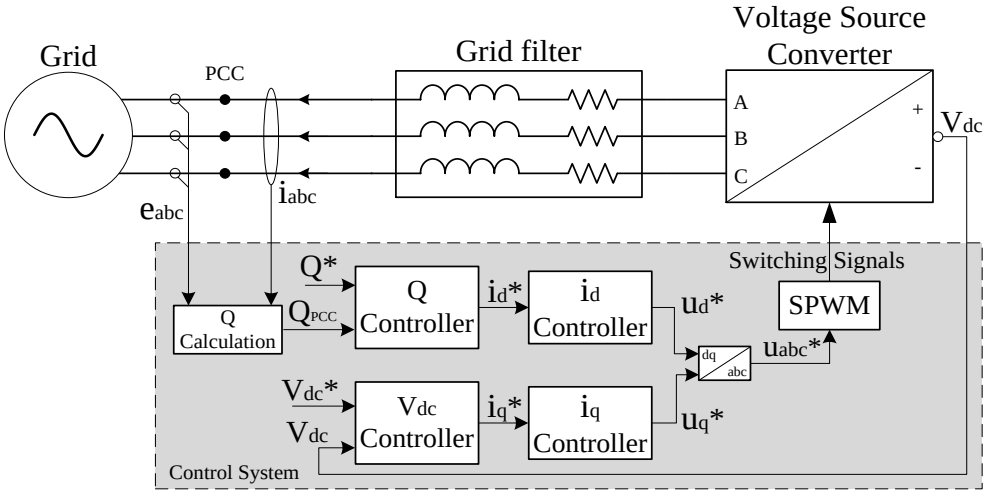


Figure 7.1. General scheme for a STATCOM application.

So, four STATCOM models have been implemented each one with one of the studied topologies. The main data for these models are summarized in Table 7.2. The reader should note that in case of MMC topology, the filter values (R-L) include also the parallel of the own converter inductances.

Table 7.2. Main data for the STATCOM models.

Nominal power	25 kVA
Grid voltage	400 V
Grid frequency	50 Hz
Grid resistance	10 μΩ
Grid inductance	1 mH
Filter resistance	25 mΩ
Filter inductance	5,5 mH
Sample time	100 μs
DC voltage reference	675 V

Concerning to the DC voltage controller, the input to be controlled in the case of MMC and CHB topologies will be the averaged value of the three sums of all modules or cells voltages in each phase. In the case of CHB the desired voltage for each cell is 675/4 V.

The modulation scheme used in all the models is the SPWM: with level-shift carriers for the NPC topologies, and phase-shifted in the case of MMC and CHB. The carrier signals frequency has been chosen in order to do two different comparisons: on one hand to compare the behavior of the different topologies using the same switching frequency for the devices, and on the other hand to obtain the same equivalent frequency in the point of common coupling (PCC). So, the switching frequency has been chosen to be 750 Hz ($m_f = 15$) for the CHB and the MMC, what results in an equivalent frequency in the PCC of 6 kHz; and for the NPC topologies the models have been simulated twice: with $f_{sw} = 750$ Hz ($m_f = 15$) and with $f_{sw} = 3$ kHz ($m_f = 60$), what results in equivalent frequencies of 1.5 kHz and 6 kHz, respectively.

In order to check the operation of the STATCOM model in each case, a reactive power reference has been fixed, being in all cases the same: 15 kVA in the first part of the simulation and -15 kVA in the second part. Note that in these models the output current of the converter is measured as positive (see Figure 7.1), so if the reactive power reference for the system is positive, it will work as a reactive power sink, or what is the same to say that it will have a capacitive behavior, consuming reactive power. Instead of this, if the reference is negative, it will generate reactive power, being a reactive power source, also known as inductive behavior.

After simulate the four models with the specified conditions, it is proved in Figure 7.2 that in all cases the reactive power follows its reference, although not in all the models the ripple of this variable is the same. It is clear to the naked eye that ANPC-based and DNPC-based STATCOMs produce reactive power with higher ripple. Table 7.3 quantifies the ripple in the different cases.

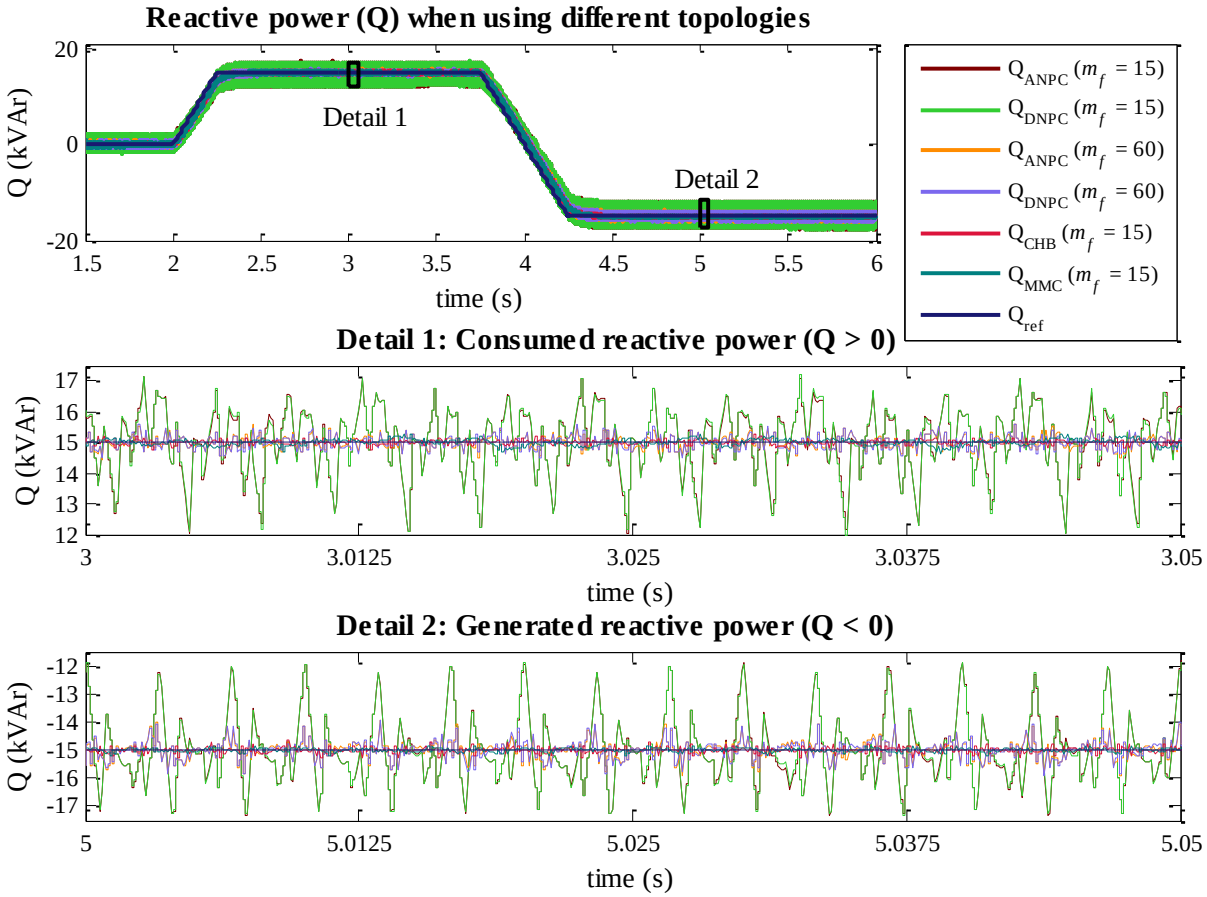


Figure 7.2. Reactive power obtained after simulate the models.

Table 7.3. Reactive power maximum ripple using the different models (kVAr).

	ANPC model (m_f = 15)	**DNPC model (m_f = 15)**	**ANPC model (m_f = 60)**	**DNPC model (m_f = 60)**	**CHB model (m_f = 15)**	**MMC model (m_f = 15)**
Q > 0	4.69 (31 %)	4.71 (31 %)	0.92 (6.6 %)	1.15 (7.7 %)	0.34 (2.3 %)	0.31 (2.1 %)
Q < 0	4.38 (29 %)	4.38 (29 %)	1.39 (9.3 %)	1.39 (9.3 %)	0.42 (2.8 %)	0.32 (2.2 %)

In relation to the signals through the PCC, there are differences using one converter or other, and also depending on the working mode of the system (if generates or consumes reactive power). Figure 7.3 shows the harmonic content of the PPC phase-to-phase voltage in the different situations, and Figure 7.4 contains the THD of the PCC current in the same cases.

Note in Figure 7.3 that the Y-axis is configured between 0 and the 25% of the fundamental harmonic, what means that the voltage harmonics amplitudes are quite low in all cases. However, seeing the current THD values it can be observed that the distortion is lower in the cases of NPC topologies working at 3 kHz than working at 750 Hz. And it also can be seen that the distortion is lower for the modular topologies than for the NPC topologies.

That peculiarity can be better observed in Figure 7.3, where the first band of harmonics in case of three-level topologies using a switching frequency of 750 Hz is around the 30th harmonic meanwhile using 3 kHz in these topologies, or 750 Hz in topologies CHB and

MMC, the first band of harmonics is around the 120th harmonic. This effect can be seen more easily when the STATCOM behaves as reactive power sink, because when it acts as a reactive power source the output voltage decreases and there is more harmonic content in it.

In the case of the modular topologies the first band of harmonics appears around the 120th because they generate nine levels voltages, and the lower harmonics are cancelled between the different modules of each phase. For the clear understanding of the previous results and their meaning, Table 7.4 contains the theoretical place where is supposed to find the first band of harmonics for each topology.

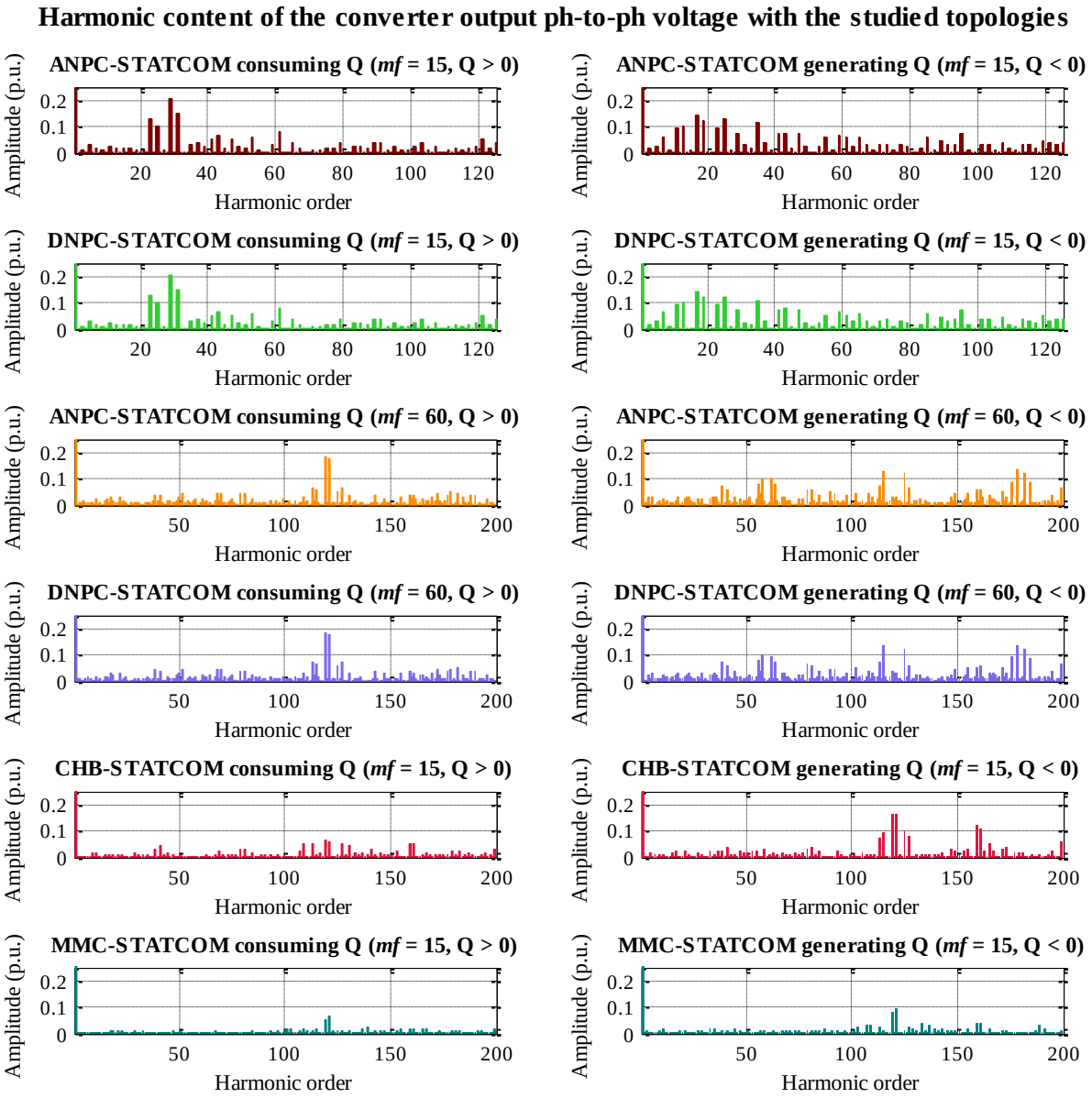


Figure 7.3. Harmonic content of the converter output phase-to-phase voltage for the different models and the two possible modes of working (generation and consumption of reactive power).

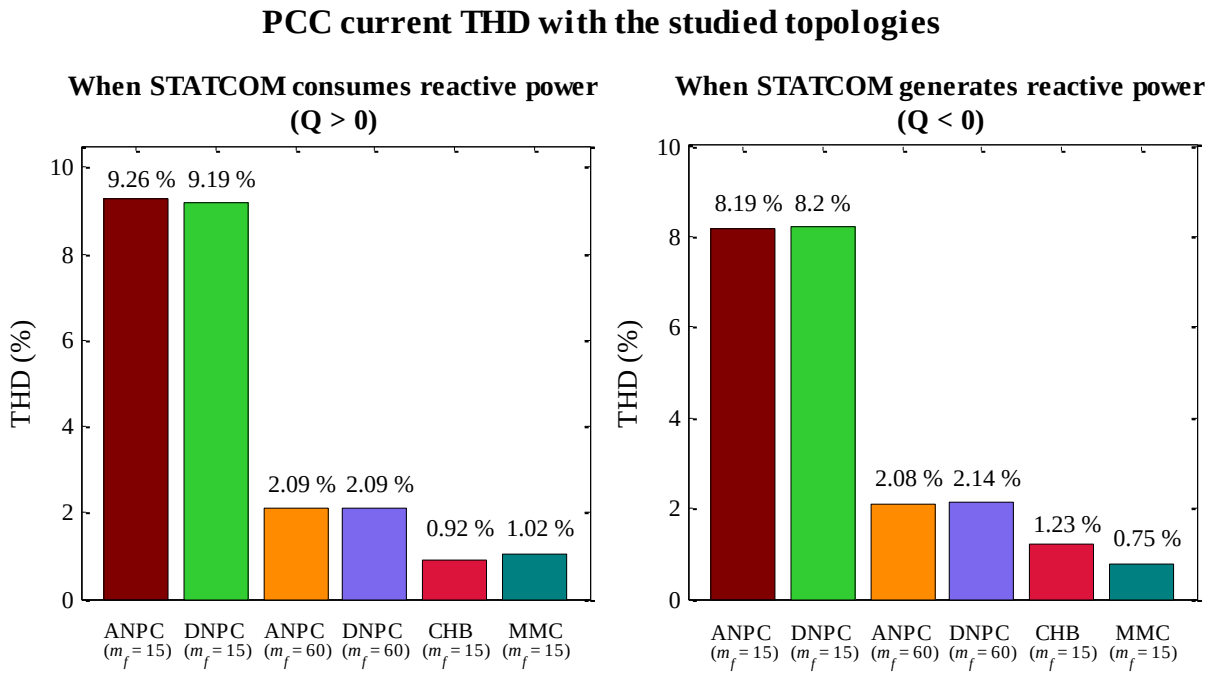


Figure 7.4. THD of the PCC current depending on the used converter and the operation mode.

Table 7.4. Theoretical place where the voltage harmonics are placed for each topology.

	ANPC model (m_f = 15)	**DNPC model (m_f = 15)**	**ANPC model (m_f = 60)**	**DNPC model (m_f = 60)**	**CHB model (m_f = 15)**	**MMC model (m_f = 15)**
Ph-to-ph voltage	Around 30th	Around 30th	Around 120th	Around 120th	Around 120th	Around 120th
Ph-to-n voltage	Around 15th	Around 15th	Around 60th	Around 60th	Around 120th	Around 120th

The losses in the power devices of the four studied topologies have been calculated from the devices voltages and currents. Analyzing these losses in the devices commutating at 750 Hz some differences can be found. In Figure 7.5 appear the losses of the devices that compose each one of the studied topologies:

- All the devices in a phase of the ANPC: S_1 to S_6.
- The active devices in a phase of the DNPC (S_1 to S_4), and the clamping diodes of this phase (D_{01} and D_{02}).
- The devices that compose one cell of the CHB: S_1 to S_4.
- The top and bottom devices of an upper submodule (SM_1), and of a lower submodule (SM_{16}).

In the case of the modular topologies, although the losses in the devices of all the cells or submodules are not shown in Figure 7.5, these losses are similar to those that are shown in

the figure. Also it is assumed that the losses in the three phases are equal. Having those premises into account, the reader can see some things:

- In the neutral point-clamped topologies the losses in the pairs of outer devices (S_1-S_4), inner devices (S_2-S_3), and clamped devices (S_5-S_6 or D_{01}-D_{02}) are similar, what means that the losses in a phase are equally distributed between the upper and lower parts.

- Also in the NPC topologies the losses in the inner devices are higher than in the outer. This fact was expected since the inner devices lead current during the zero state/states and the outer do not.

- The losses in the NPC topologies are similar in the case of inner and outer devices, but in the case of DNPC the losses in the clamped diodes are much higher than the clamped devices of ANPC. This fact increases a lot the total losses of the DNPC converter.

- In the CHB converter the losses in all the devices that compose a single cell are similar. Due to the phase-shift modulation is applied the losses are almost equal for all the cells (for clarity reasons in Figure 7.5 only the losses in one cell have been shown).

- In MMC the reader should note that, as the strategy N+1 is used and in each moment the number of activated submodules is the same, the average losses in an upper arm submodule (in this case SM_1) and in a lower arm submodule (SM_{16}) is similar. Note than the difference between the losses in top and bottom devices is due to the used modulation index.

- Comparing the four topologies total averaged losses (Figure 7.6) it can be seen that DNPC topology generates the highest losses due to the clamping diodes. Moreover these losses are not evenly spread between its devices. The same happens with ANPC converter, its losses are not well distributed over all the devices. This is a disadvantage compared to the modular topologies as it contributes to the unequal ageing of the devices.

- Of course, the losses shown in Figure 7.5 and Figure 7.6 are from the simulation results and hence they don’t include some other losses that real prototypes layout could produce.

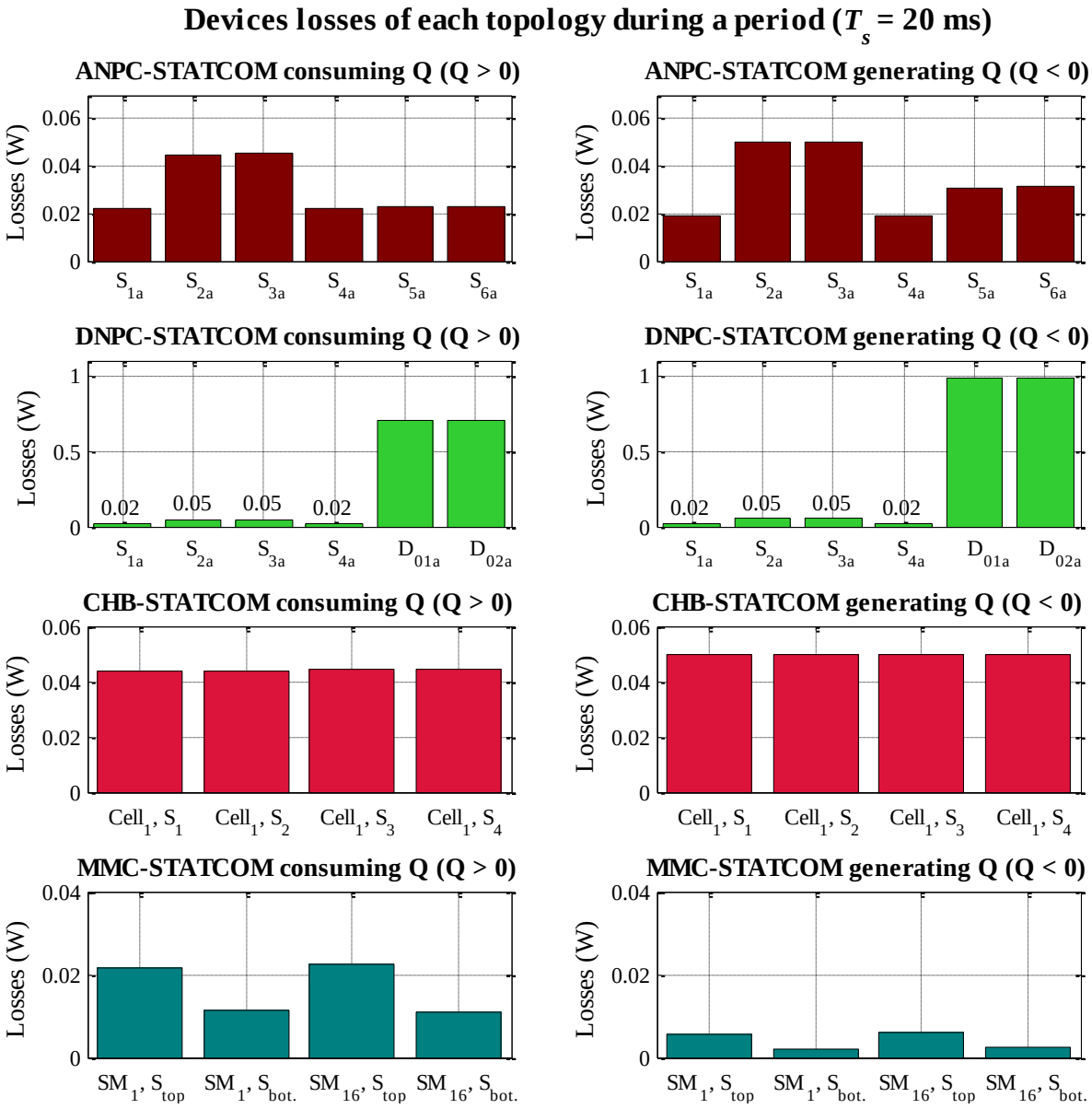


Figure 7.5. Losses in the devices of each one of the studied topologies.

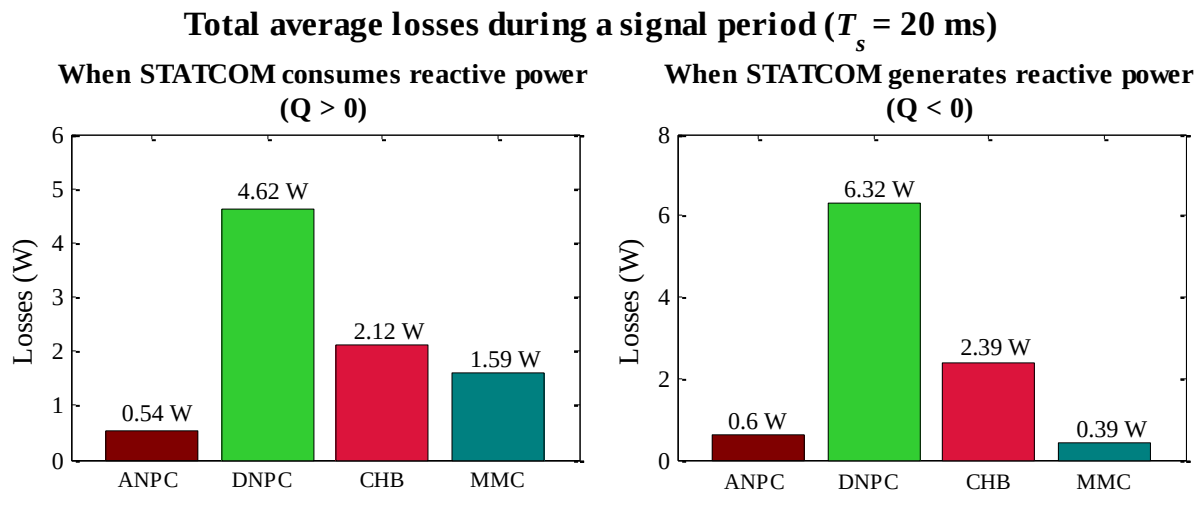


Figure 7.6. Total average losses of the studied topologies during a period of the grid signal.

7.2.2. Induction motor drive simulation models

In a similar way than in the previous case, a 3L-ANPC, a 3L-DNPC, a 9L-CHB (4-cells per phase), and a 9L-MMC (16-submodules per phase) have been compared when are used in an induction motor drive system.

The description and operation of an induction motor drive is described in detail in Appendix C. In this case the motor is controlled with indirect field oriented control (FOC), such as is depicted in Figure 7.7. Basically, the implemented drive works as follows: the speed controller gets the speed reference value and generates the proper reference values for torque and flux. These values are sent to the flux oriented controller that is responsible of checking if the motor is magnetized, and also generates the corresponding references for the stator current *dq*-components. The requested current values are processed through the current controller that generates the voltage reference (v_{abc}*). These voltage references are normalized with the DC voltage value in each case, and they are used to generate the switching signals for the converter. Note that the voltage references normalization in the case of the cascaded H-bridge converter is done following the explanation done in subsection 4.4.3.

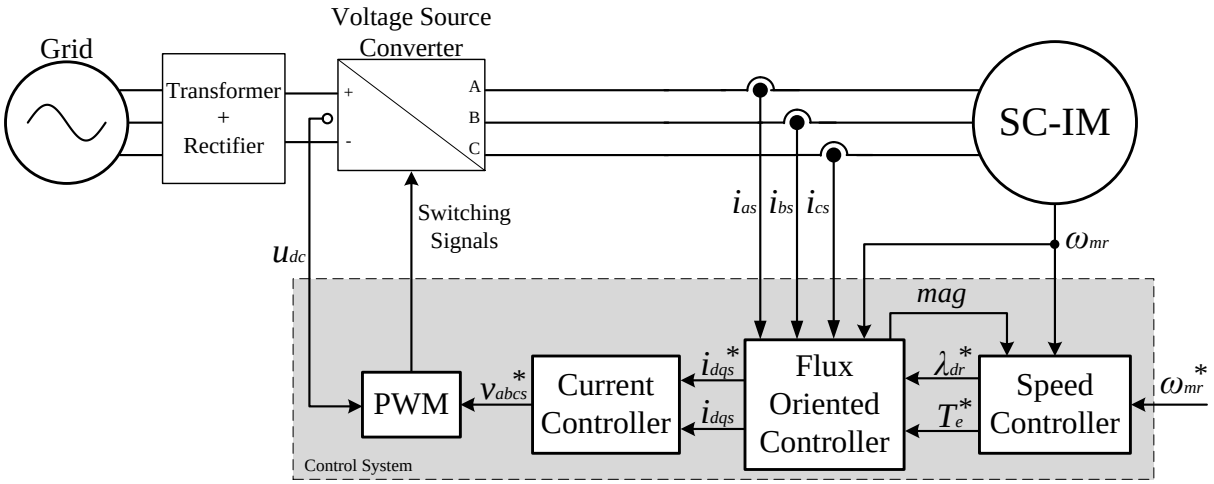


Figure 7.7. General scheme for an induction motor drive controlled with indirect FOC.

The four models of induction motor drive with the different topologies have been implemented with the same characteristics that are summarized in Table 7.5. In order to feed the different converters multi-pulse transformers have been used. The transformer characteristics are also summarized in Table 7.5. In the case of NPC topologies and the MMC converter the secondary windings are connected with the corresponding rectifiers, and then the DC voltages are connected in series in order to obtain a DC supply with low ripple. For having more details of this operation see Appendix A.

And, as in the case of the STATCOM models, the modulation scheme used in all cases is the SPWM: with level-shift carriers for the NPC topologies, and phase-shifted in the case of MMC and CHB converters. As happened in the previous case, the CHB and MMC models have been simulated with a switching frequency of 750 Hz ($m_f = 15$), and the neutral

point-clamped models have been simulated twice: with switching frequency of 750 Hz (m_f = 15), and 3 kHz (m_f = 60). This is done in order to compare the differences between the resultant equivalent frequencies in each case.

Table 7.5. Main data for the drive models.

Sample time		100 μs	
Induction Machine		Siemens 1LA 163-4AA	
Nominal power		11 kW	
Nominal voltage		690 V	
Nominal current		12.4 A	
Poles		4	
Nominal speed		1460 rpm	
Nominal torque		72 Nm	
Multi-pulse transformer			
For ANPC, DNPC and MMC		**For CHB**	
Voltage	400/125 V (4 windings)	**Voltage**	400/125 V (12 windings)
Connection		**Connection**	
Primary	400 V – Star	Primary	400 V – Star
Secondary	Delta – 30º (1 winding) Z-1 – 15º (1 winding) Star – 0º (1 winding) Z-2 – (-15º) (1 winding)	Secondary	Delta – 30º (3 windings) Z-1 – 15º (3 windings) Star – 0º (3 windings) Z-2 – (-15º) (3 windings)

With the purpose of checking the operation of the motor drive models, both speed and torque references have been fixed, being the same in all cases. Those references change along the simulation time to emulate both spinning directions. Figure 7.8 shows the motor speed and torque obtained after simulate all the models in the previous conditions. As it can be seen in the figure both variables follows their references in all the cases. In order to illustrate the torque controller dynamics one of the transitions has been enlarged; and it can be seen how in the case of the MMC the controller is slightly slower than in the other cases, and it has also more oscillations.

In relation to the motor voltages, there are differences using one converter or other, and also depending on the frequency modulation index stablished. Figure 7.9 shows the harmonic content of the motor phase-to-phase voltage in the different situations, and Figure 7.10 contains the THD of the motor current in the same cases.

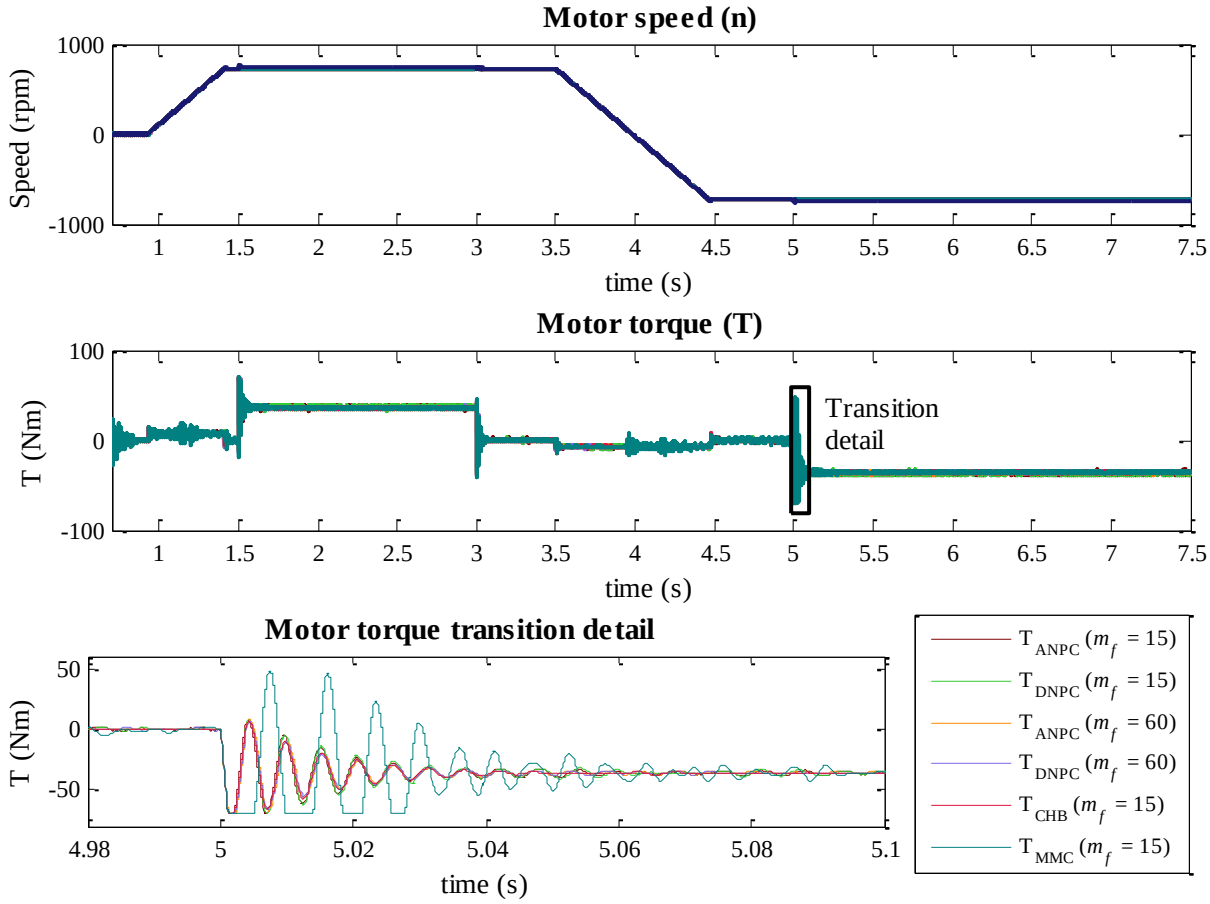


Figure 7.8. Motor speed and torque obtained after running the models.

It can be seen in Figure 7.9 how the first band of harmonics appears around the 30th harmonic in the case of NPC topologies with $m_f = 15$, and around the harmonic 120th in the rest of cases. That is because the equivalent output frequency in the modular topologies is 3 kHz. It can be also appreciated in that figure how the first band of harmonics in the cases of CHB and MMC is composed of a higher number of harmonics with less amplitude than in the case of NPC topologies working with $m_f = 60$. This effect was explained in Figure 4.10 and Figure 5.5. In all cases the harmonics in the second band have greater amplitudes than in the first one.

Figure 7.10 shows that the current THD is higher in the case of NPC topologies controlled with $m_f = 15$ (the same as in the STATCOM models), that is because in those cases the harmonics are closer to the fundamental one and they have higher amplitudes.

In this case the losses comparison has not be shown because the losses distribution is similar to the case of STATCOM models.

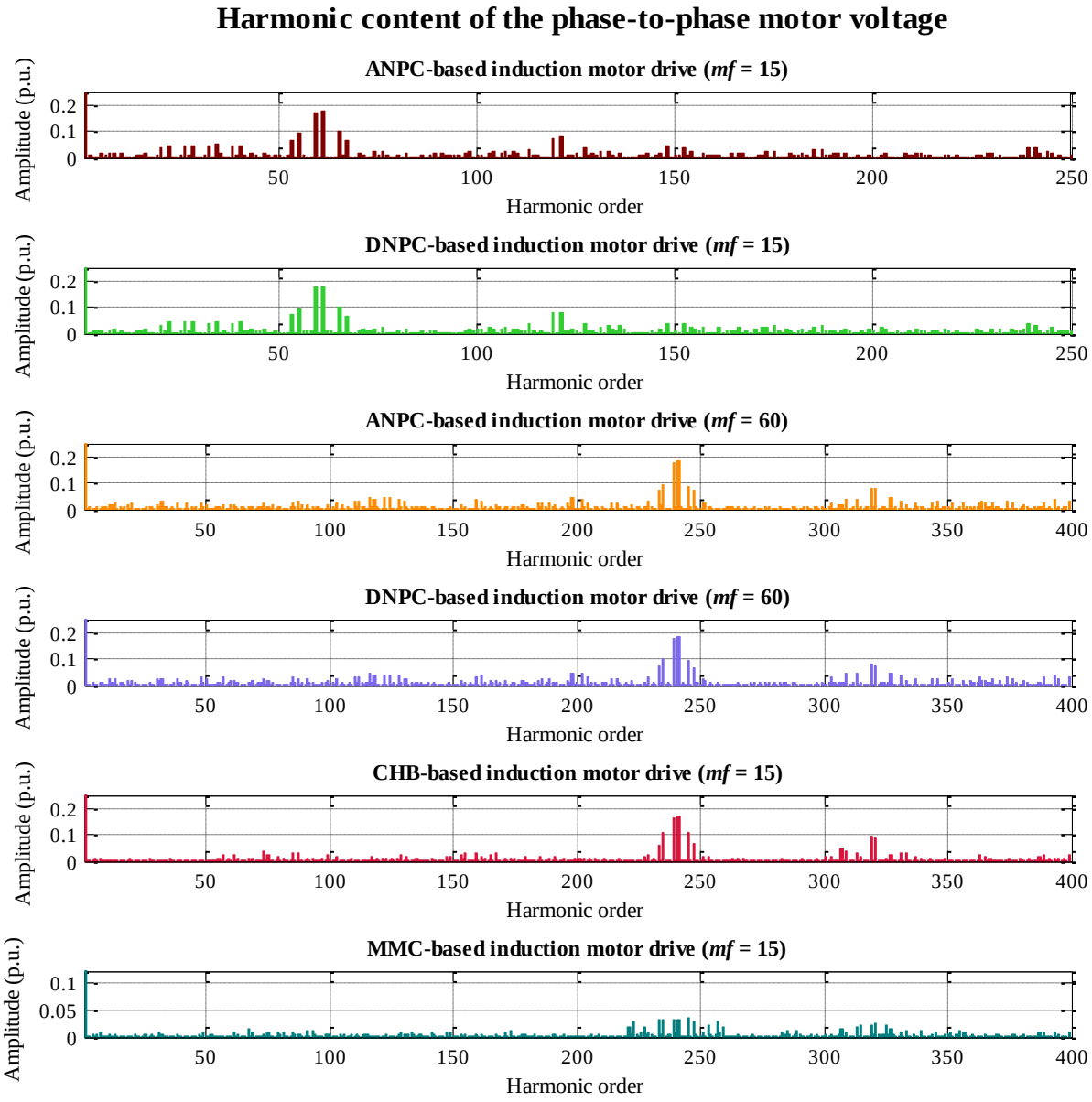


Figure 7.9. Harmonic content of the motor phase-to-phase voltage for the different models.

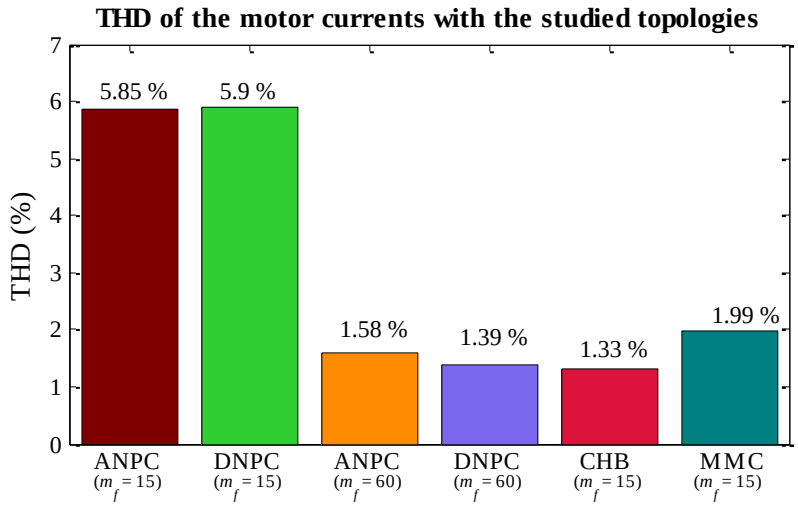


Figure 7.10. THD of the motor currents for the different models.

7.3. Results

7.3.1. Simulation results of fault-tolerant CHB-based drive

The neutral-shift balancing method proposed in subsection 4.3.4 has been modeled and included in a simulation of a 4-cells CHB-based drive for an induction motor controlled with indirect field oriented control. The detailed explanation of the induction machine and its controllers can be found in Appendix C, and a block diagram of the system implemented in this case is depicted in Figure 7.11. The implemented drive works in a similar way than in the previous case: the speed controller generates the reference values for torque and flux, which are sent to the flux oriented controller that generates the corresponding references for the stator current *dq*-components. The current controller process the reference current values and generates the voltage reference (V_{ref}). The requested voltage reference is then sent to the shaded block depicted in Figure 7.11. This block generates the proper modulation signals according to the neutral-shift balancing method explained in subsection 4.3.4, and these modulation signals are compared with the carrier ones to generate switching pulses for each cell of the Cascaded H-Bridge converter.

The main data of this model are summarized in Table 7.6.

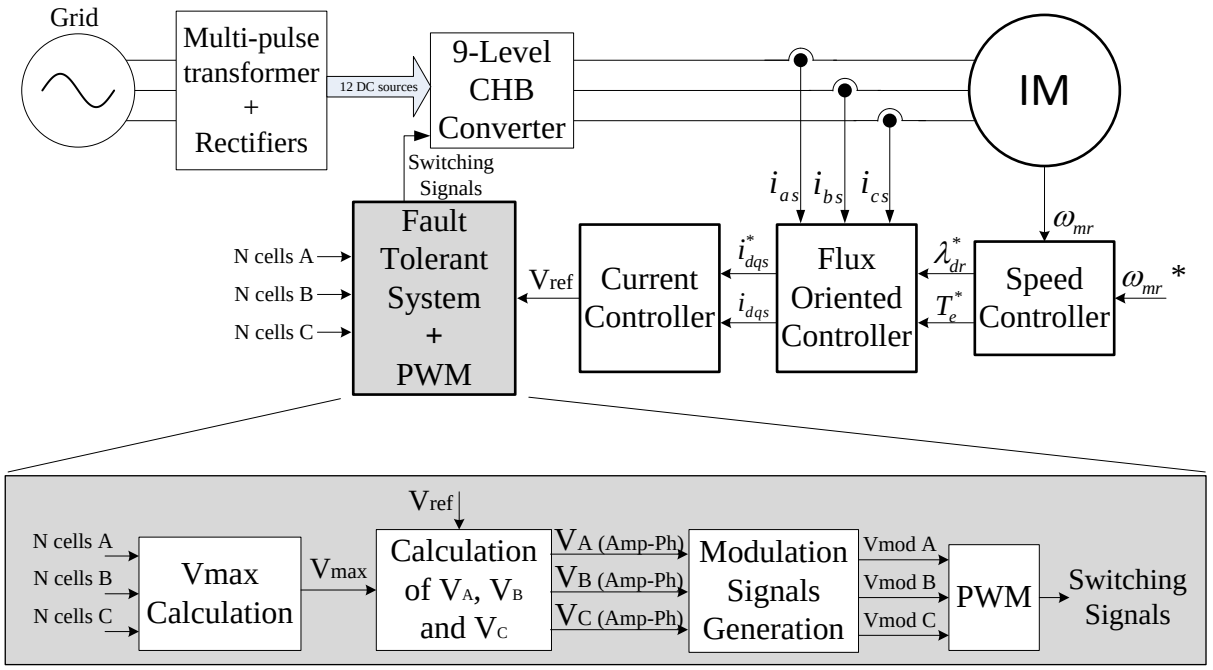


Figure 7.11. Block diagram of the fault-tolerant CHB-based drive modelled.

In order to check the effectiveness of the proposed algorithm some tests have been done. Specifically the model has been simulated with all its cells operative, that represent its normal operation, and also it has been simulated bypassing one, two and three cells. According to that, Figure 7.12 shows the phase-to-phase voltages and currents that are supplied by the CHB converter to the motor in normal operation (phase A in blue, phase B in green, and phase

C in red). These signals are represented for the case in which any balancing method is applied, and for the case of the balancing method application. Of course, in the case of Figure 7.12, as all cells are operative, both situations are equal. Figure 7.13 represents the same voltages and currents in the case of fault in cell C1, and Figure 7.14 and Figure 7.15 represent respectively the cases of failure in B1 and C1, and failure in B1, C1 and C2. As the reader can see as the number of faulty cells increases the proposed method effectiveness become more evident. In order to quantify the imbalance in the voltage and currents supplied to the motor, the following formulas are used:

$$Imbalance_v = \frac{\left|{v_{dq}}^{neg}\right|}{\left|{v_{dq}}^{pos}\right|} \cdot 100\% \tag{7.1}$$

$$Imbalance_i = \frac{\left|{i_{dq}}^{neg}\right|}{\left|{i_{dq}}^{pos}\right|} \cdot 100\% \tag{7.2}$$

The equations (7.1) and (7.2) represent the ratios between the negative sequence and the positive sequence of voltage and current. This is true if the speed sign is positive, in case of change in the direction, the ratio will be the opposite relationship (between positive sequence and negative sequence).

Table 7.6. Main data of the fault-tolerant CHB-based drive with indirect FOC control.

Grid	400 V 50 Hz	
Multi-pulse transformer	50 kVA 400/125 V (12 windings)	
	400 V – Star	125 V – Delta – 30º (3 windings)
		125 V – Z-1 – 15º (3 windings)
		125 V – Star – 0º (3 windings)
		125 V – Z-2 – (-15º) (3 windings)
Induction Motor (Siemens 1LA 163-4AA)	11 kW 690 V (Y connection) 1460 rpm	

The imbalance in the cases represented from Figure 7.12 to Figure 7.15 has been quantified and the results have been summarized in Table 7.7. In this table it can be seen how the imbalance of both voltages and currents is lower when the proposed balancing method is applied, in comparison to not applying any method.

Table 7.7. Quantification of the voltage and current imbalance for the cases of normal operation, and for the cases of fault in C1, in B1 and C1, and in case of fault in B1, C1 and C2.

	Normal Operation (Figure 7.12)		**Fault in C1 (Figure 7.13)**	
	Without any method	**With proposed method**	**Without any method**	**With proposed method**
V imbalance	0.82 %	1.24 %	4.35 %	2.38 %
I imbalance	1.3 %	1.33 %	13.47 %	1.58 %
	Fault in B1 and C1 (Figure 7.14)		**Fault in B1, C1 and C2 (Figure 7.15)**	
	Without any method	**With proposed method**	**Without any method**	**With proposed method**
V imbalance	3.07 %	1.21 %	9.09 %	0.80 %
I imbalance	15.45 %	2.74 %	43.01 %	3.53 %

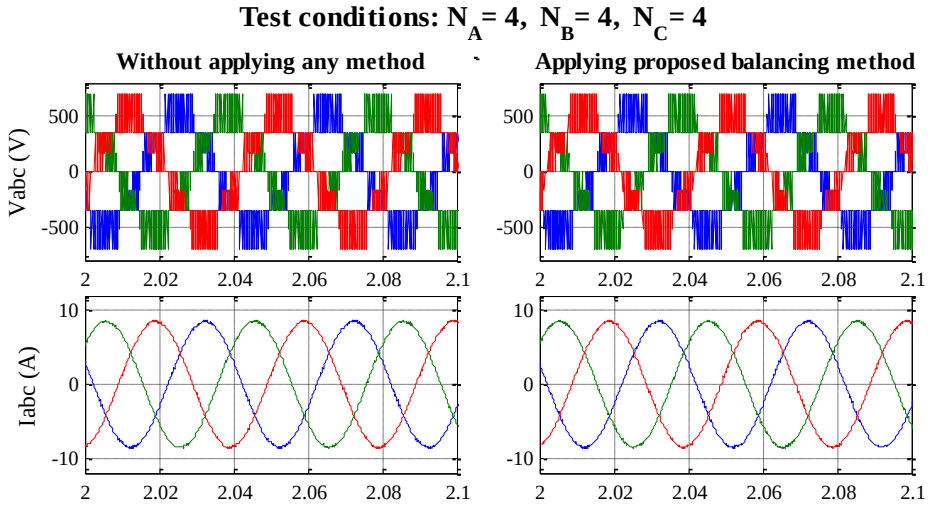


Figure 7.12. Phase-to-phase voltages and currents supplied to the motor in normal operation.

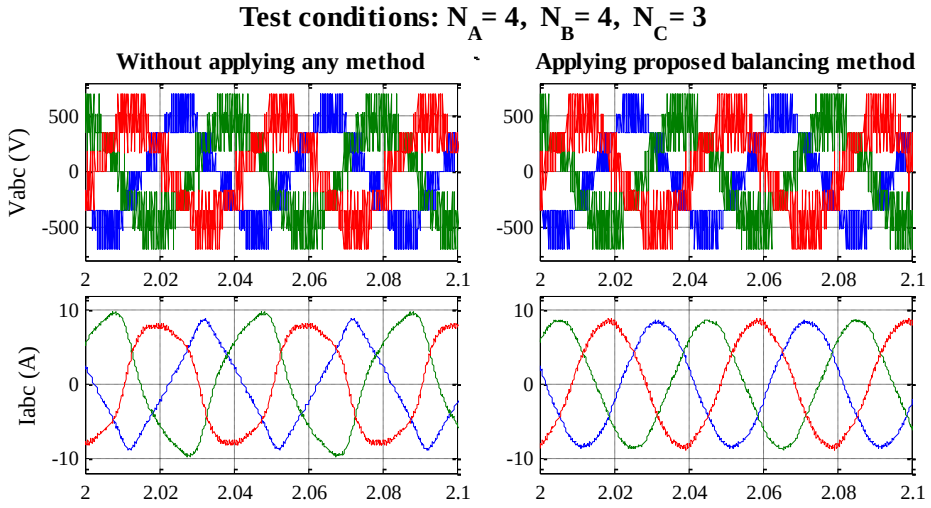


Figure 7.13. Phase-to-phase voltages and currents supplied to the motor in case of fault in C1.

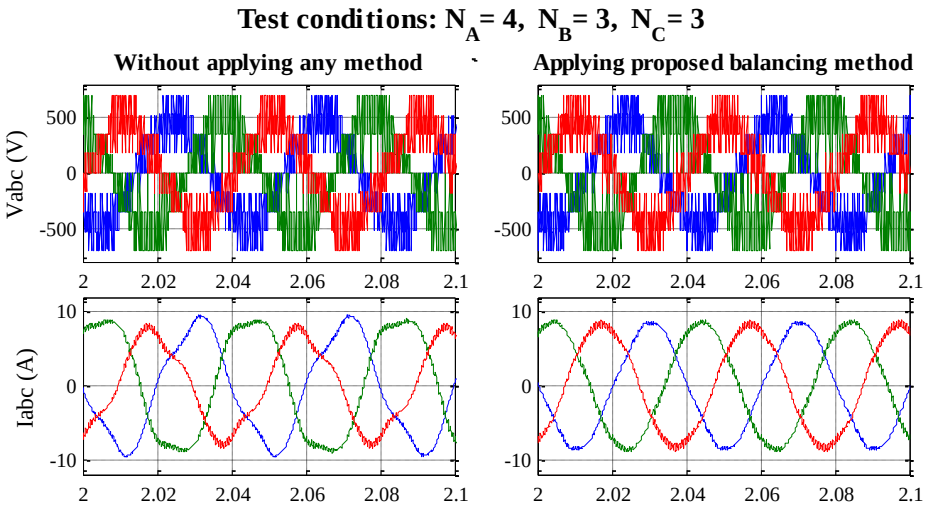


Figure 7.14. Phase-to-phase voltages and currents supplied to the motor in case of fault in B1 and C1.

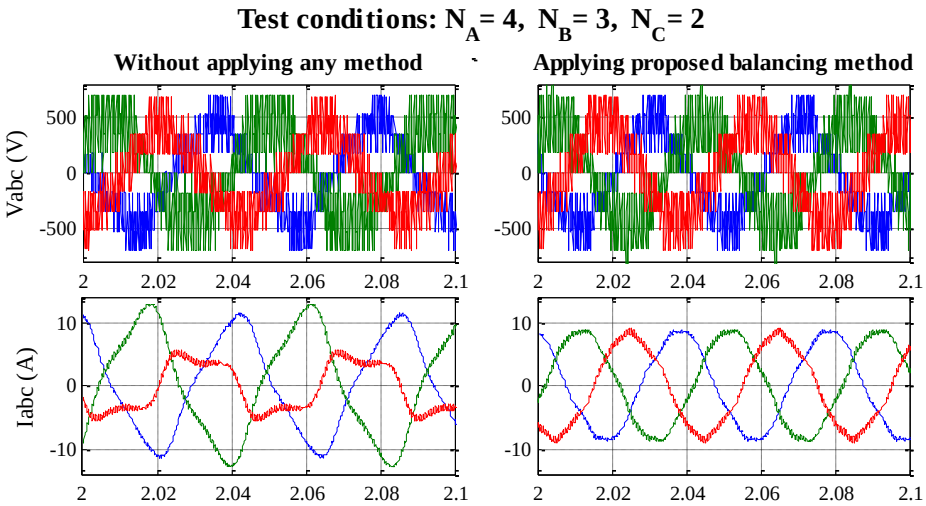


Figure 7.15. Phase-to-phase voltages and currents supplied to the motor in case of fault in B1, C1 and C2.

7.3.2. Experimental results

In this subsection some experimental results obtained in laboratory tests will be summarized. First of all, the proposed neutral-shift modulation method has been tested. In order to assure the correct operation of the modulation method, it has been implemented in the control platform composed by dSPACE system and an FPGA-based board (as explained in subsection 6.2.2), and then it has been used to control the CHB prototype.

In this case, for these results the prototype has been connected to a resistive load of 7 kW. However, as the maximum voltage for the load is 400 V (phase-to-phase rms value), and the maximum voltage that can supply the CHB prototype is around 825 V, a transformer with a relation of 828/400 V has been connected between the converter output and the load in order to not damage any element. As it can be seen in Figure 7.16, in Figure 7.17, in Figure

7.18, and in Figure 7.19, a third harmonic injection has been done in all the modulation signals. The modulation indexes are: $m_f = 15$; $m_a = 0.83$. The signals acquired in the tests are the converter output currents (depicted in the upper side of the figures) and the phase-to-neutral output voltages of the converter (shown in the lower side).

In all the mentioned figures it can be seen how the fault-tolerant method allows supplying to the load a balanced set of voltages (and hence, of currents). The quantification of this balance can be seen in Table 7.8, and it is compared with the case not using any balancing method.

Table 7.8. Voltage imbalance quantification of the balancing method applied to the CHB converter that feeds a 7 kW resistive load.

	Normal operation	**Fault in C1**	**Fault in B1 and C1**	**Fault in C1 and C2**	**Fault in B1, C1 and C2**
Without applying any method	0.99 %	7.64 %	9.49 %	18.63 %	18.34 %
Applying the proposed fault-tolerant method	0.58 %	5.98 %	6.58 %	4.03 %	8.28 %

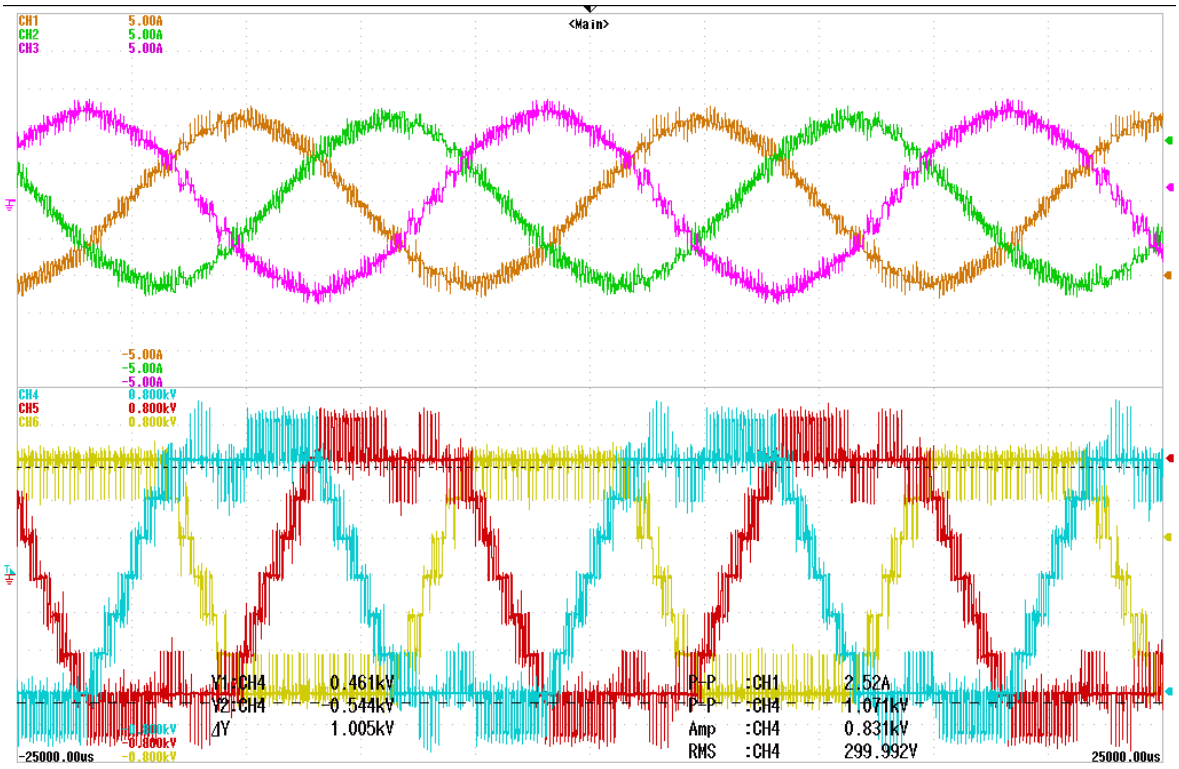


Figure 7.16. Application of the proposed neutral-shift balanced method when the CHB prototype is feeding a resistive load of 7 kW and there is a fault in C1. The figure shows the converter currents (up) and the converter phase-to-neutral voltages (down).

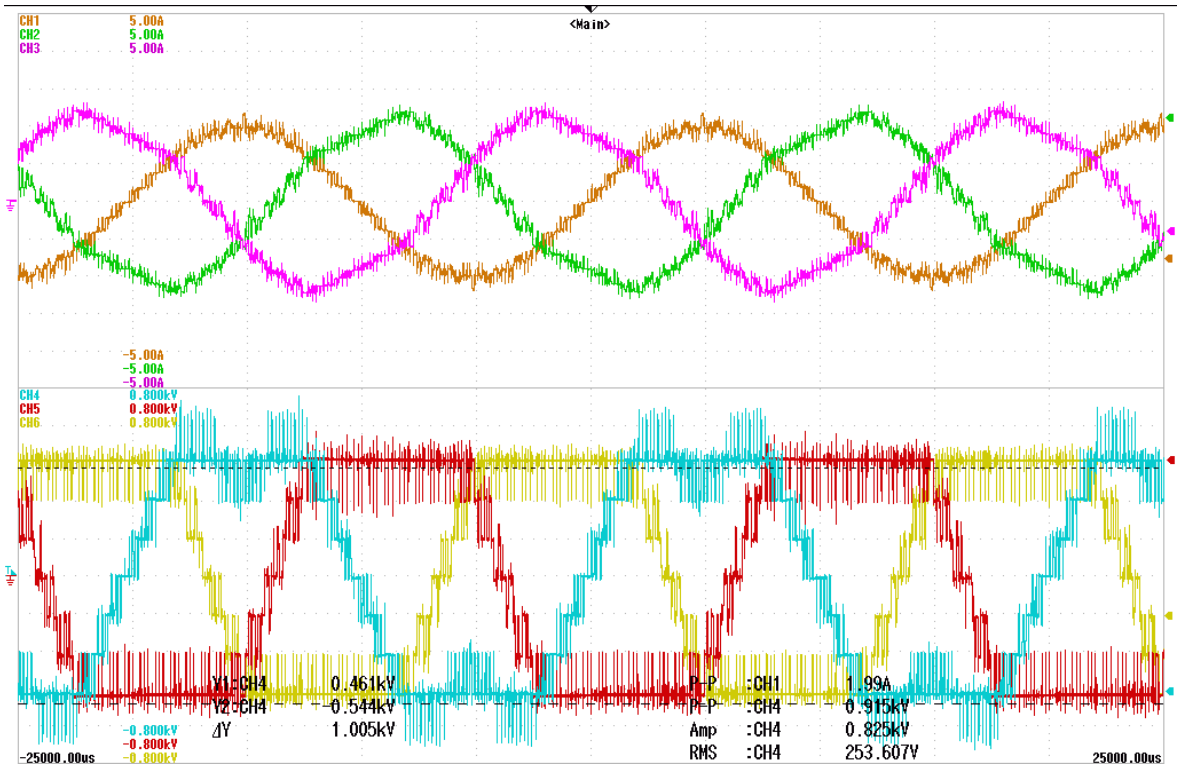


Figure 7.17. Application of the proposed neutral-shift balanced method when the CHB prototype is feeding a resistive load of 7 kW and B1, and C1 have faults. The figure shows the converter currents (up) and the converter phase-to-neutral voltages (down).

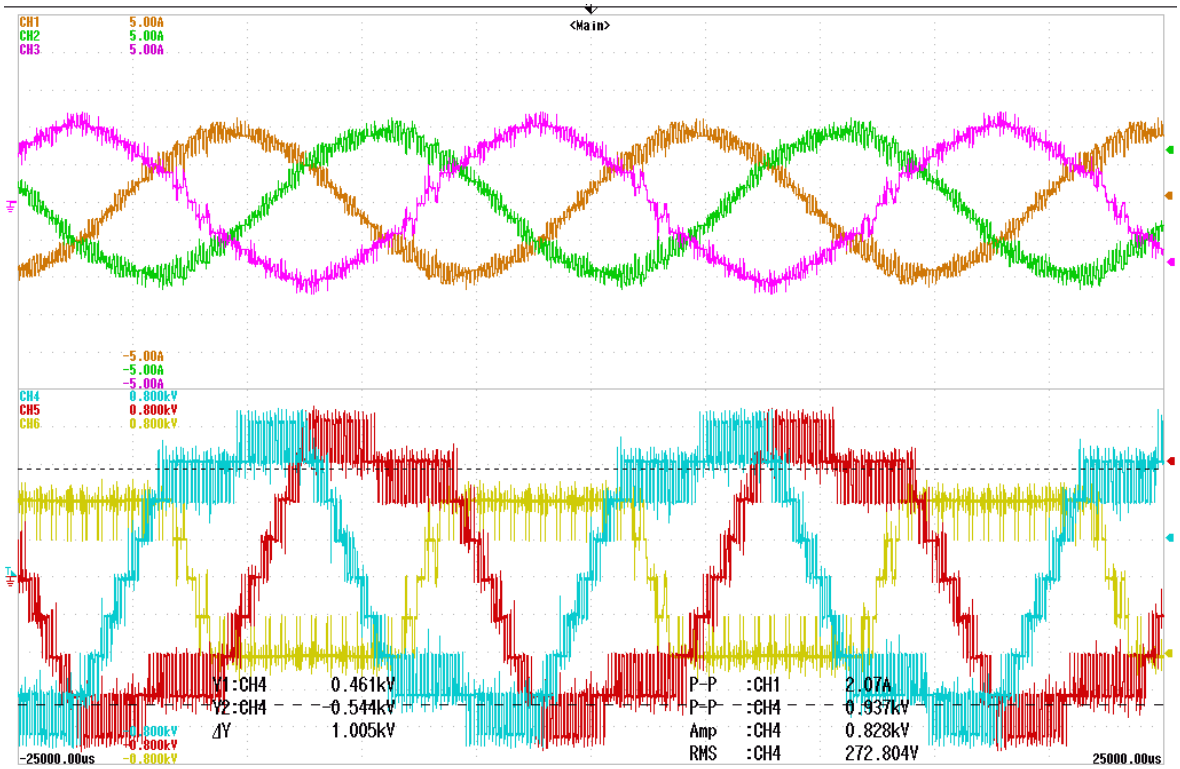


Figure 7.18. Application of the proposed neutral-shift balanced method when the CHB prototype is feeding a resistive load of 7 kW and C1, and C2 have faults. The figure shows the converter currents (up) and the converter phase-to-neutral voltages (down).

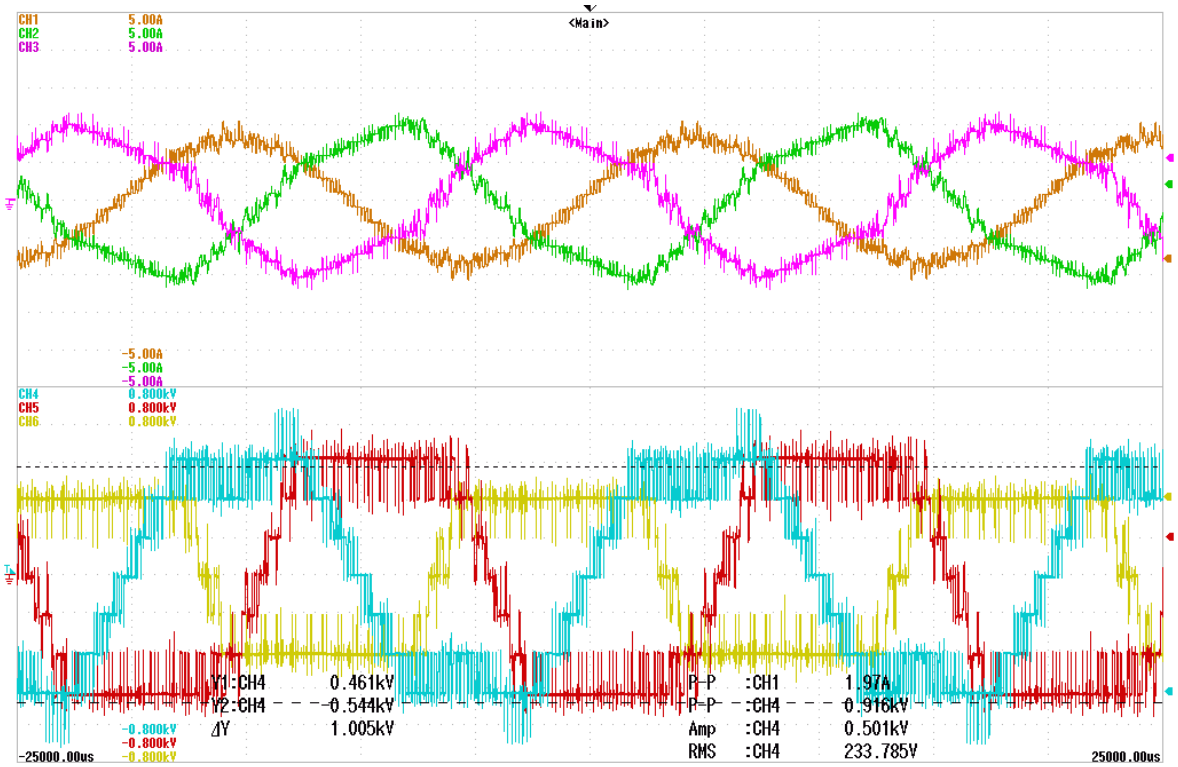


Figure 7.19. Application of the proposed neutral-shift balanced method when the CHB prototype is feeding a resistive load of 7 kW and B1, C1, and C2 have faults. The figure shows the converter currents (up) and the converter phase-to-neutral voltages (down).

After the tests in the CHB converter, some results have been obtained testing the DNPC and the MMC prototypes in STATCOM application.

Specifically the diode neutral point-clamped converter detailed in section 6.1 has been testing as a part of a STATCOM system, so, in this case the back-to-back connection is not used, and only the grid-connected converter has been used.

The test has been done with a reactive power reference of 15 kVAr, and a switching frequency of 2.5 kHz. In this case the phase-to-phase voltages and the currents in the point of common coupling have been acquired with a sampling frequency of 5 kHz. These signals are shown in Figure 7.20, and their harmonic content has been calculated and it is depicted in Figure 7.21.

The harmonic content of these signals can be quantified through the value of the total harmonic distortion. In this case the THD value for the PCC current in the DNPC-based STATCOM is (considering the harmonics up to the 50^{th}):

$$\mathrm{THD}i = 8.79\ \% \tag{7.3}$$

On the other hand, the MMC described in section 6.4 has been tested as a part of a STATCOM system working with a switching frequency of 750 Hz. The system has been tested fixing a reactive power reference of 20 kVAr, and the phase-to-phase voltages and

currents in the PCC have been acquired with a sample frequency of 10 kHz. These signals are represented in Figure 7.22, and their harmonic content is shown in Figure 7.23. As the reader can see in Figure 7.22, and especially in Figure 7.23, these signals have a very low harmonic content. This fact is proved if its current THD is calculated (the harmonics up to the 100th):

$$\mathrm{THD}i = 1.37\ \% \tag{7.4}$$

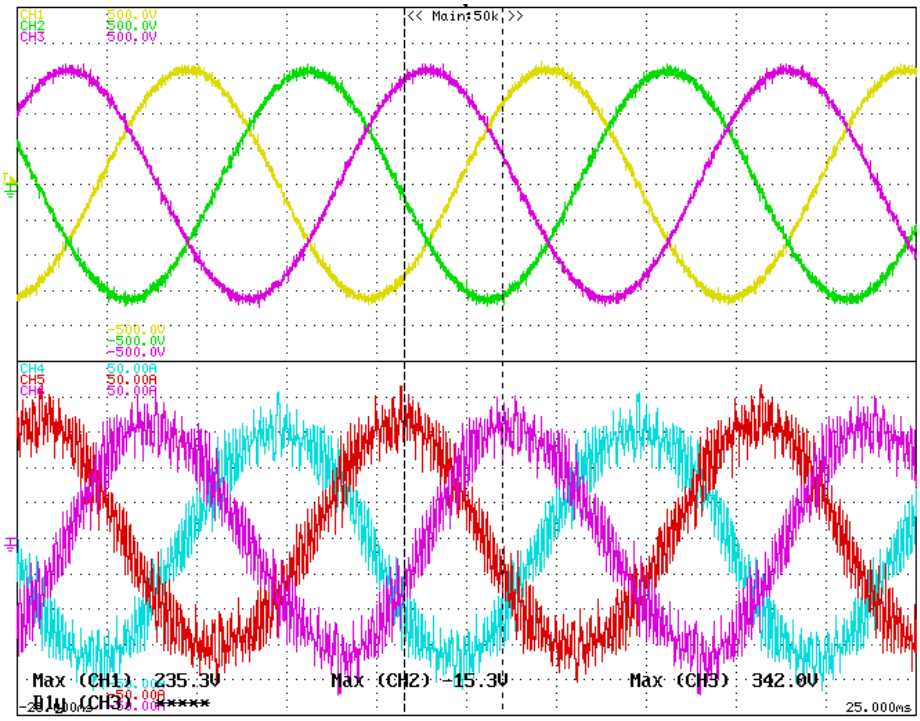


Figure 7.20. Illustration of the PCC phase-to-phase voltages and currents in the DNPC-based STATCOM.

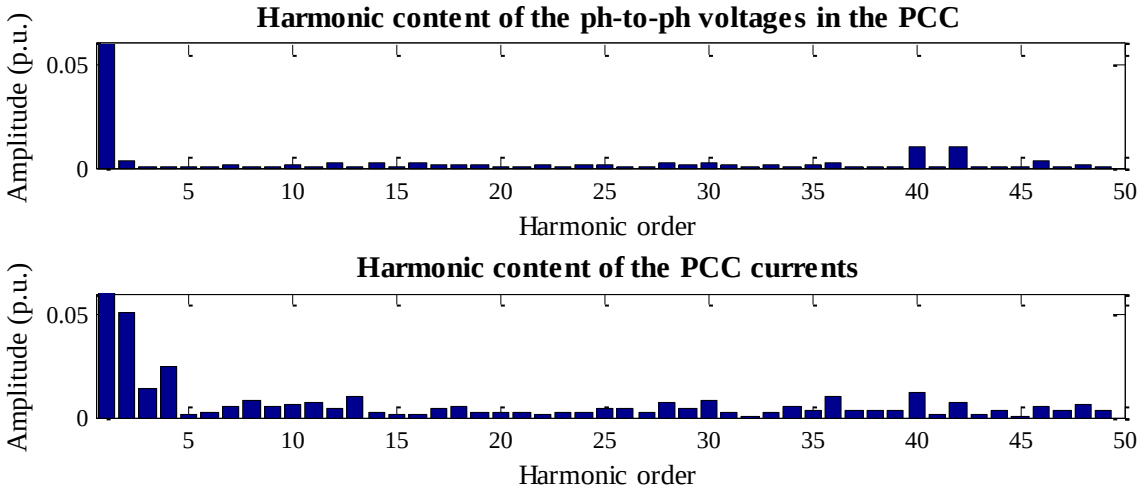


Figure 7.21. Harmonic content of the PCC voltages and currents of the DNPC-based STATCOM.

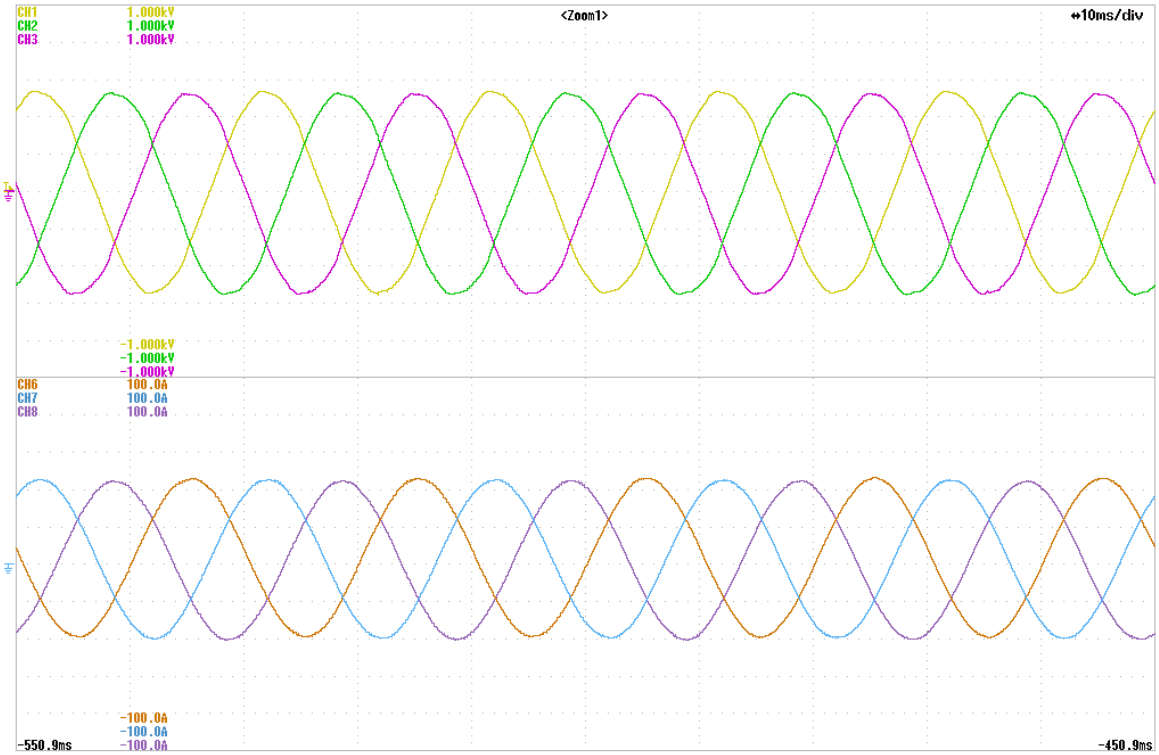


Figure 7.22. Illustration of the PCC phase-to-phase voltages and currents in the MMC-based STATCOM.

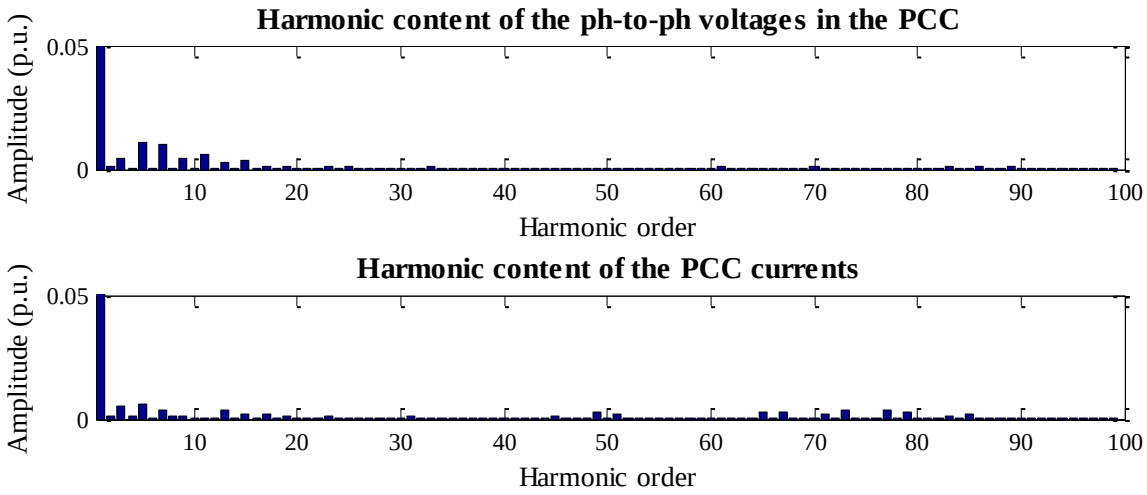


Figure 7.23. Harmonic content of the PCC voltages and currents of the MMC-based STATCOM.

To conclude the experimental results, some tests have been done to check the operation of the six-cells, thirteen-levels CHB converter designed by the company *Sedecal Control*, which was explained in section 6.3.

As this prototype is not finished yet, the tests have been done in low voltage instead of medium voltage. In this case the eighteen cells have been fed with independent DC sources at 55 V. Figure 7.24 shows an example of the phase-to-phase voltage and the phase-to-neutral voltage at the converter's output.

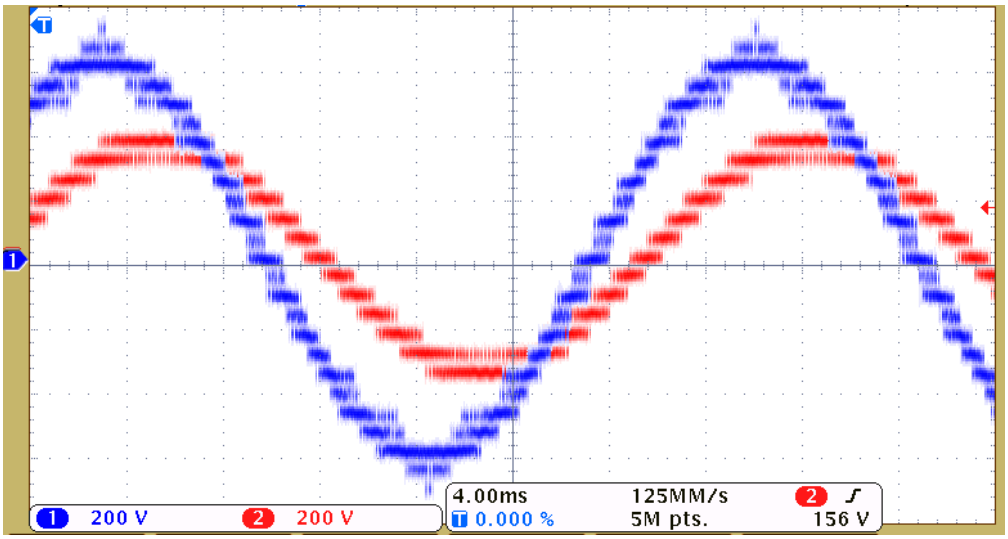


Figure 7.24. Illustration of phase-to-phase voltage (yellow) and phase-to-neutral voltage (cyan) in the converter's output.

The converter is connected to an induction motor with nominal power of 65 kW, nominal voltage of 400 V (Y), nominal current of 124 A, and nominal speed of 730 rpm. The motor is controlled through a *v/f* controller, where a reference of 500 rpm is fixed. Figure 7.25 and Figure 7.26 show two examples of the evolution of currents and phase-to-phase voltages in the converter's output when the mentioned controller is applied. It can be seen how the voltage increases at the same time as the frequency.

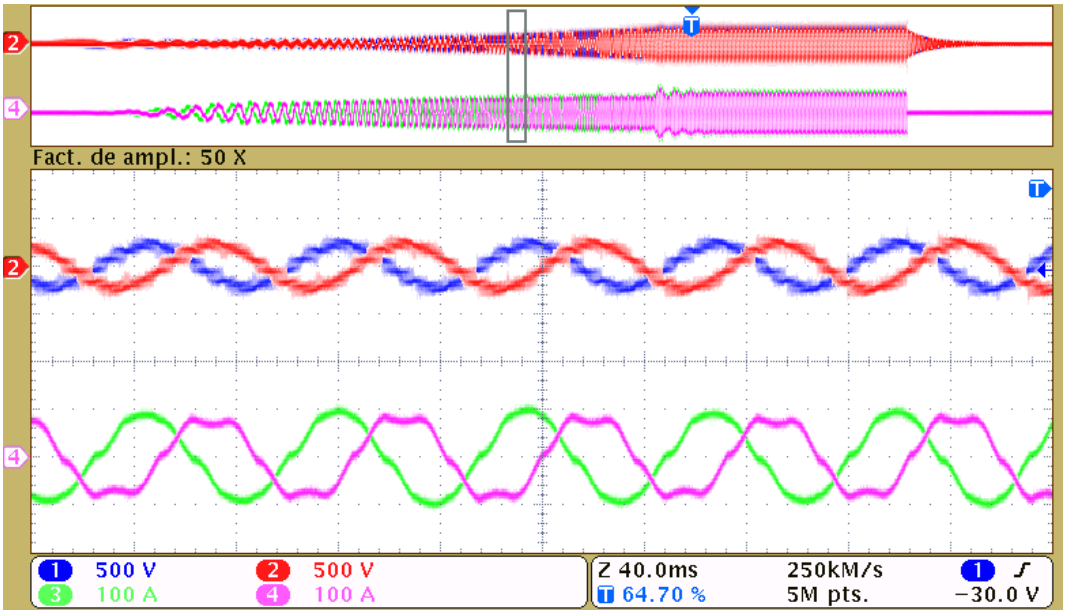


Figure 7.25. First example of the evolution of the phase-to-phase voltages (v_{AB} and v_{BC}) and currents (i_A and i_B) when a voltage-frequency controller is applied to the described prototype.

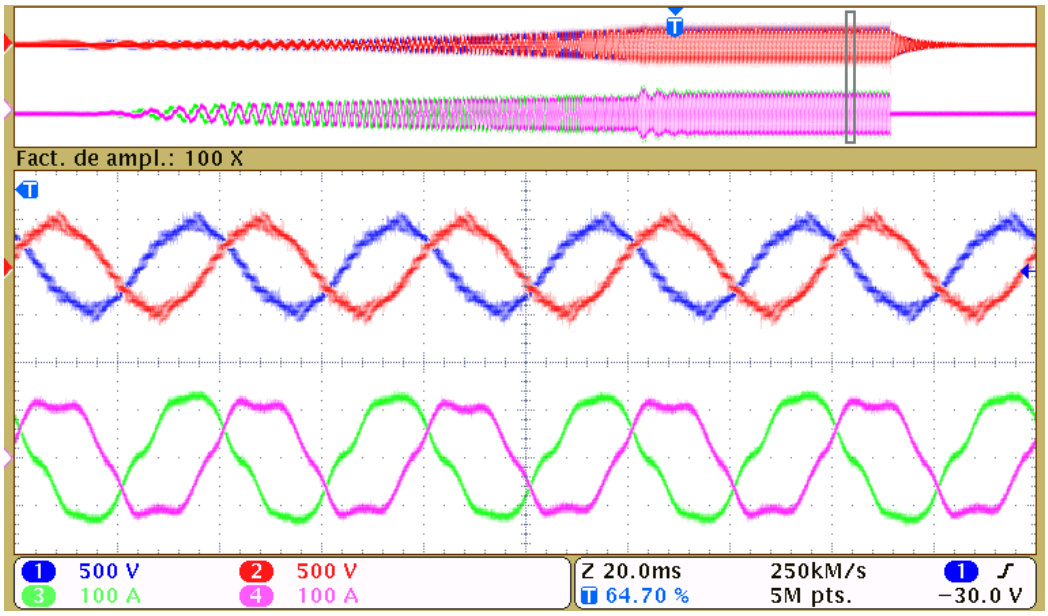


Figure 7.26. Second example of the evolution of the phase-to-phase voltages (v_{AB} and v_{BC}) and currents (i_A and i_B) when a voltage-frequency controller is applied to the described prototype.

7.4. Conclusions

After analyzing the results obtained with the previous test some conclusions can be drawn. The first of them is that with the modular topologies like CHB or MMC it is possible to obtain a higher number of levels in the signals, as in NPC topologies this number is limited to three. Hence, modular topologies are more employed in higher voltage applications.

From the point of view of the voltage range the NPC topologies are a very good option for applications up to 3300 V. Above this voltage it will be needed a modular topology. The optimal application range for a unidirectional CHB converter is for its use in high-power motor drives and the highest range of medium-voltage. On the other hand, the MMC is an optimal system for very high-voltage, for which it was designed. For the medium-voltage applications like the analyzed in this Thesis is also a good option but reducing the number of submodules. Note that for very high-voltage applications each submodule switch can be composed by up to eight IGBTs, but in the applications analyzed in this Thesis each switch is composed by one low-voltage IGBT.

Regarding to the control systems, the optimal solution in applications up to 3300 V is the NPC topologies because can be controlled with centralized systems. However, in drive applications it will be necessary expensive filters in order to reduce the dv/dt. The modular topologies require more complex wiring and acquisition system that in case of high number of modules probably will tend to be a distributed control system. These distributed systems will need specific dedicated buses, as the commercial ones are not suitable for this purpose.

From the point of view of the application in which the topologies are implemented, for power quality applications like STATCOM systems all the studied options are suitable, only

the NPC topologies are limited by the voltage range. In renewable generation like for example offshore wind connections the NPC topologies using back-to-back configuration are a very good option. In higher voltage bidirectional applications like multi-terminal DC connections the only option is to use MMC converters. And for the highest range medium-voltage drives the best option is the CHB topology.

Another consideration to have into account is the possibilities to have fault-tolerant behavior. That can be achieved working with the modular topologies, but the only topology that really has an active neutral point is the CHB converter.

Summarizing what is explained above, Figure 7.27 shows the comparison of some of the main characteristics of the analyzed topologies. The figure represents the differences between the topologies: regarding to the voltage range, as was said previously, the NPC topologies are limited, and the MMC is the topology that can reach higher voltages; but nevertheless, the current range in NPC topologies is higher because usually the maximum current of the devices is related with the maximum voltage, and for these converter is needed to use high-power devices. The number of devices is clearly higher in the modular topologies than in the ANPC or DNPC, and for the same number of levels, the MMC converter needs double devices than the CHB topology. In terms of equivalent frequency, in the case of NPC topologies it is directly related with the switching frequency; in the case of modular topologies, the equivalent frequency (for a fixed switching frequency) grows with the number of modules, which allows enlarge devices life-time. Regarding to the fault-tolerant operation, it is almost impossible in the NPC topologies, and easier for the modular topologies: in the case of CHB is needed to implement a voltage balancing method, and in the case of MMC the balance is done automatically, although is advisable to control the THD increase.

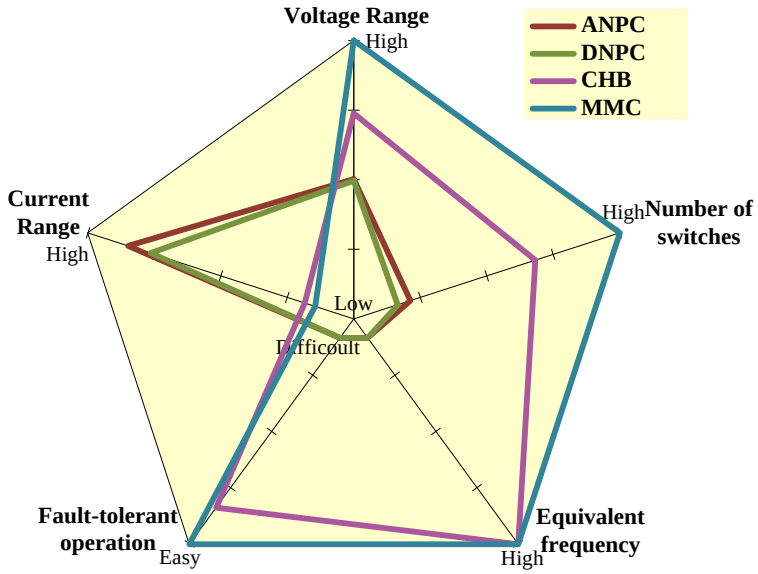


Figure 7.27. Illustration of some of the main characteristics of the analyzed topologies.

To conclude, it worth to mention that ANPC converter has a critical issue that needs an intense analysis. This is the optimal losses distribution and current path choosing due to the parasite inductances generated by the zero states.

Chapter 8: CONCLUSIONS AND FUTURE WORKS

This chapter contains the conclusions obtained after the realization of this work, and also it summarizes the proposed future works.

8.1. Conclusions

This Thesis is focused in study four of the most used multilevel topologies in our days. These topologies have been studied separately and then, they have been compared attending to different criteria.

A complete study of each topology has been done, analyzing the modulation techniques typically employed for each one. Special emphasis has been placed on the modulation based on selective harmonics elimination. This method has been studied for the four chosen topologies, and several sets of angles solutions have been calculated.

Moreover, when this modulation method is implemented in the active neutral point-clamped converter the zero states should be chosen in advance, and in this work an alternative proposal of zero states choice has been done in order to balance the conduction and switching losses among the devices of each half of a phase.

Regarding to the operation after a device fault, the possibility of keeping the operation has been studied for each topology. Unfortunately, the neutral point-clamped topologies do not have any options apart from the devices redundancy that supposes a cost increment. In this sense, the modular topologies give more options for adapting the operation to the fault condition:

- For the cascaded H-bridge converter some methods for balancing the output phase-to-phase voltages after a fault have been studied. Moreover, an analytical

neutral-shift method has been proposed in this Thesis for achieve this purpose. This method has been implemented and testing in simulation models and also in the real CHB prototype sited in the GEISER laboratory with satisfactory results.

- In the case of the modular multilevel converter the options are reduced. As there is a single DC source for all the phases, it is impossible to apply a neutral-shift method. As an advantage, the DC voltage is shared among the non-faulty submodules; the only requirement is to maintain even the number of submodules in each phase. In case of fault in a submodule of an MMC, the situation is that one of the phases has less levels in its output voltage than the other two phases. This fact may produce current distortion. In order to avoid this effect in this work a rearrange of the carrier signals for the remaining submodules is done.

The medium voltage applications in which the four chosen topologies are usually implemented have been analyzed, and as a conclusion for this analysis, the suitable topology for each application has been selected:

- The NPC topologies are suitable for any medium-voltage application up to the range of 3300 V. Above this range it will be necessary using a modular topology than can reach higher voltage.

- MMC converters are the optimal option in system with very high-voltage, for which they were designed. For the analyzed medium-voltage applications they are also suitable but reducing the number of submodules.

- The CHB topology is optimal for its use in high power motor drives in the highest range of medium voltage. Moreover, the possibility to do this topology fault-tolerant through one of the balancing methods explained in this Thesis is a great advantage.

The modulation and control methods analyzed in this Thesis for the different topologies have been tested in simulation models and also in real prototypes in the laboratory. One of the prototypes, the cascaded H-bridge converter, has been designed and developed completely during this Thesis by this author and her mentor.

After this summary, it can be concluded that all the objectives of this Thesis work have been achieved.

8.2. Future works

In order to complete the tasks performed during this Thesis, some future works are proposed:

- Obtaining experimental results working with higher voltages in order to approximate the results to an industrial scale. The aim of this work will be checking

if the implemented algorithms and controllers are valid for an industrial application. Although all the modulation methods and controllers have been designed to be easily adaptable to medium voltages, it is important to verify experimentally this point.

- Comparative study of the right sizing of reactive components for the studied topologies. In this work the sizing of reactive components such us the DC capacitors that all topologies need, or the inductances proper of the MMC converter have not been studied in detail, but this is an interesting issue that is proposed for the future.

- Study of the cascade H-bridge converter operation to allow a bidirectional behavior. The usual operation of CHB converter fed through a multi-pulse transformer and rectifiers do not allow the bidirectional behavior. The reason is that the rectifiers are usually not-controlled. However if controlled rectifiers are used, it is possible the bidirectional behavior although it would need special considerations to control those rectifiers.

- Detailed analysis of the peculiarities that has the implementation of selective harmonic elimination in systems with closed-loop control. This is an interesting issue as using SHE supposes working with low switching frequencies, and this fact implies the adaptation of the rest of controllers in the system. Most of the times this adaptation consists on make lower the controller sample time.

- Implementation of the control methods designed in hardware platforms with digital processors. For example, for the implementation of the proposed the neutral-shift method, as it has a considerable mathematical complexity, the explained simplifications can be applied.

- Development of multi-terminal direct current (MTDC) grids based on modular multilevel converters. The control of MTDC connections is an important research topic for DC grid technologies manufacturers, offshore transmission networks developers, and grid system operators that have or are planning to have VSC DC links connected to their system, or who contemplate being part of a DC grid in the future. In this kind of grids MMC converter will be the chosen topology, as its development will be a good solution for the implementation of advanced control for autonomous power sharing, frequency support, or protection in MTDC grids, as an example.

- Study of modulation methods that allow the reduction of common-mode voltages. The normal operation of converters in medium voltage drives produces common-mode voltages due to the switching action of the semiconductor devices in the converter. If not mitigated, the common-mode voltages are superimposed on the motor voltages and cause the premature failure of this element. Traditionally, the problem was solved by introducing an isolation transformer between the utility grid

and the converter, but it will be very interesting to study the possibility of achieving this mitigation through the modulation methods.

- Study of the roles that will have the medium voltage converters in the future electric grids based on power electronics. The electric grids are tending to be increasingly smarter and more efficient, and it is foreseeable that for this issue the power converters will play an important role.

Appendix A: MULTI-WINDING, PHASE-SHIFTING, AND MULTI-PULSE TRANSFORMERS DESIGN

The objective of this appendix is to lay the groundwork to understand how the multi-pulse transformers are useful to operate power electronics applications, especially to feed cascaded H-bridge converters, or non-linear loads.

The first step is to make clear concepts like multi-winding transformers or phase-shifting transformers, in order to understand the behavior of this kind of hardware and how they are used to achieve the final aim: the multi-pulse transformer.

So, in this appendix the basis of multi-winding transformers and phase-shifting transformers are explained, and after that, it is detailed how to design a multi-pulse transformer depending on the desired application.

A.1. Multi-winding transformers

A multi-winding transformer is defined as a transformer that has more than one winding in its primary or in its secondary side, as shown in the example of Figure A.1. The principle of operation in these transformers is not different from the ordinary ones, and turns and voltages ratios are calculated in a similar way. The principle is the following: the primary winding, or windings (in the case that are more than one), provides magnetic flux that is transmitted to the secondary winding or windings through the iron core (see Figure A.2).

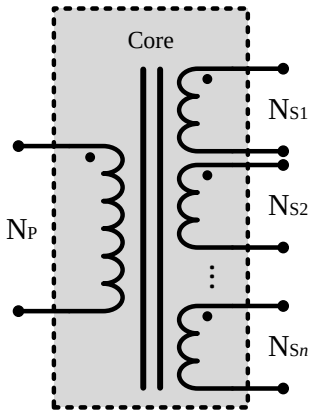


Figure A.1. Example of monophasic multi-winding transformer with one winding in the primary side and n windings in the secondary side.

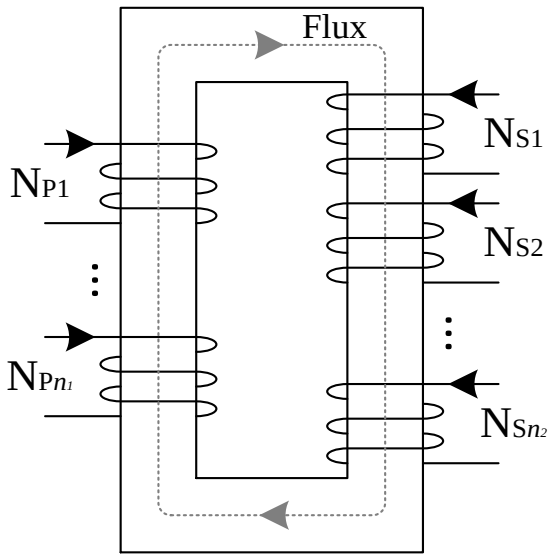


Figure A.2. Representation of the magnetic flux induced by the n_1 primary windings to the n_2 secondary windings.

As in multi-winding transformers operates the principal of mutual induction (as in conventional transformers), and all windings are associated to the same core, the reader can see that the ratio volts per turn is the same in all of windings, although not all of them have necessarily to have the same nominal voltage, as not all of them have to have the same number of turns.

The multiple windings in a multi-winding transformer can be used separately or can be connected together. In this last case, it must be paid specially attention to the dot convention in order to respect the voltage polarities.

Figure A.1 and Figure A.2 illustrate examples of monophasic transformers, but there are also three-phase multi-winding transformers.

A.2. Phase-shifting transformers

The term phase-shifting transformer makes reference to that transformer in which the phase-to-phase voltages in the secondary side have different orientation that the voltages in the primary side. So, this term includes the typical connections wye/delta or vice versa, but is specially applied to those connections that allow a configurable shift between primary and secondary sides, which are known as zig-zag connections.

In the traditional wye/delta or delta/wye connections there is a shift of 30º between primary and secondary sides. The shifting angle, δ, is defined as:

$$\delta = \angle\overline{V}_{ab} - \angle\overline{V}_{AB} \tag{A.1}$$

where $\overline{V}_{AB}$ and $\overline{V}_{ab}$ are the phasors that represent the phase-to-phase voltages of primary and secondary sides respectively.

Figure A.3 shows an example of this connection, and it can be seen that the phase-to-phase voltage in the secondary side has a leading phase angle of 30º with respect to the primary side (δ = 30º). In the case that a 30º lagging angle is needed (δ = –30º), it can be used the delta/wye connection.

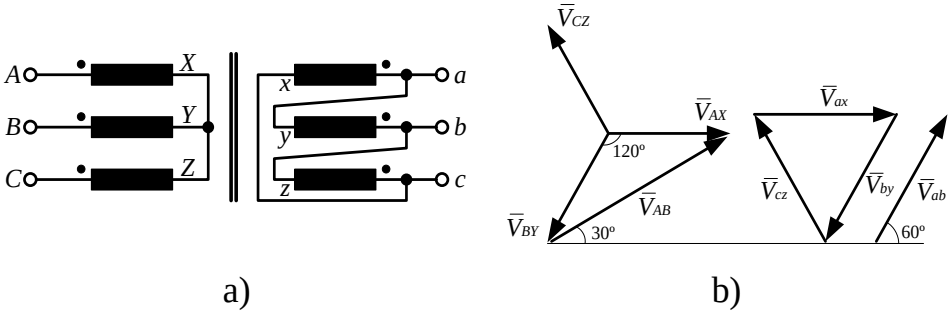


Figure A.3. Representation of a wye/delta connection a), and its phasor diagram b).

As said previously, if shifting angles different from 30º are needed other connections must be used. Those connections are known as zig-zag, and they can be used to obtain leading or lagging angles. Usually this kind of transformers have the primary winding (N_1 turns per phase) connected in wye or delta, and the secondary side divided in two windings (N_2 and N_3 turns per phase) that are connected in zig-zag as it will be explained in the following subsections. Calculating carefully N_2 and N_3, and connecting them properly, the desired phase shifting between primary and secondary is achieved.

A.2.2. Leading angle transformers (connection Y/Z-1)

Leading angle transformers are those transformers that generate an advanced shift between the voltage angles of the secondary and the primary sides, what is the same to say those transformers that generate a positive δ.

The configurable positive angle is achieved connecting the primary winding in wye with N_1 turns per phase, and dividing the secondary winding in two coils per phase with N_2 and N_3 turns respectively. N_2 coils are connected in delta and then in series with N_3 coils. This connection is known as zig-zag (Z-1) and is represented in Figure A.4.a). As it is depicted in this representation, the rms voltages in coils N_2 and N_3 are named v_P and v_Q respectively.

The phasors diagram corresponding to this connection is shown in Figure A.4.b). Considering the triangle enclosed by the phasors $\overline{V}_{ab}$, $\overline{V}_{by}$, and $\overline{V}_Q$, and applying the sin theorem the following relationship is find:

$$\frac{V_Q}{\sin(30° - \delta)} = \frac{V_{by}}{\sin(30° + \delta)} \tag{A.2}$$

where $0° \leq \delta \leq 30°$, and V_{by} is the rms phase voltage between points *b* and *y*. As in balanced three-phase systems V_{by} is equal to V_{ax} and to V_{cz}, equation (A.2) can be rewritten as:

$$\frac{V_Q}{V_{ax}} = \frac{\sin(30° - \delta)}{\sin(30° + \delta)} \tag{A.3}$$

From equation (A.3) the turns ratio of the secondary winding coils can be calculated as

$$\frac{N_3}{N_2 + N_3} = \frac{V_Q}{V_{ax}} = \frac{\sin(30° - \delta)}{\sin(30° + \delta)} \tag{A.4}$$

so, for a desired value of δ the ratio N_3 to (N_2 + N_3) can be obtained.

Similar to equation (A.2), the relationship between V_{ab} and V_{by} can be calculated:

$$\frac{V_{ab}}{\sin 120°} = \frac{V_{by}}{\sin(30° + \delta)} \tag{A.5}$$

From which it can be deduced the following

$$V_{ax} = V_{by} = \frac{2}{\sqrt{3}} \sin(30° + \delta)\, V_{ab} \tag{A.6}$$

The turn ratio between primary and secondary windings is

$$\frac{N_1}{N_2 + N_3} = \frac{V_{AX}}{V_{ax}} \tag{A.7}$$

Having into account that $V_{AB} = \sqrt{3} V_{AX}$, and substituting equation (A.6) into (A.7), it is obtained the relationship between the coils and the desired angle, δ:

$$\frac{N_1}{N_2 + N_3} = \frac{1}{2\sin(30° + \delta)} \frac{V_{AB}}{V_{ab}} \tag{A.8}$$

Examining the two extreme cases, it can be seen that if the coil N_2 is reduced to zero, the secondary winding shown in Figure A.4 becomes a wye connection, and V_{AB} and V_{ab} have the same phase (δ = 0). In the opposite case, if N_3 is zero, the secondary winding would be in delta connection and δ would be 30º. So the phase-shifting angle for the Y/Z-1 connection is in the range of 0º to 30º.

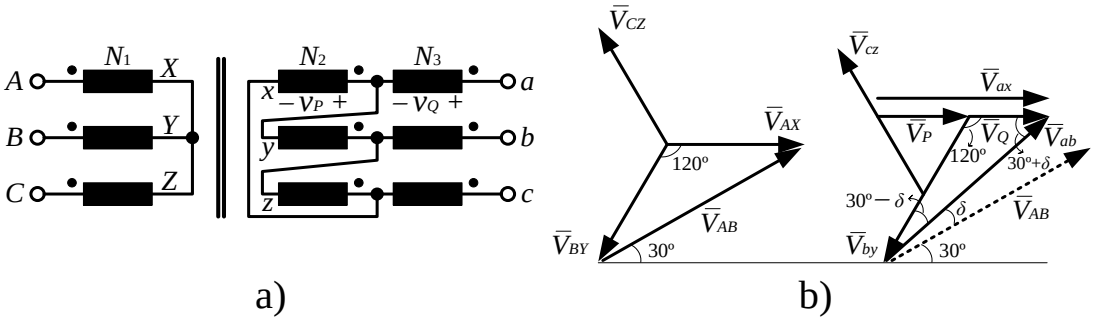


Figure A.4. Representation of Y/Z-1 connection a), and its phasors diagram b).

A.2.3. Lagging angle transformers

There are some connections that allow achieving a configurable lagging angle between the primary and secondary windings. In this subsection three connections that meet this objective will be shown: Y/Z-2, Δ/Z-1, and Δ/Z-2.

A.2.3.1. Connection Y/Z-2

The connection Y/Z-2 is similar to connection Y/Z-1, but in this case the secondary coils N_2 are delta-connected in reverse order than in the previous case. This connection is shown in Figure A.5.

From phasors diagram in Figure A.5.b), and following a similar procedure to that explained in equations from (A.2) to (A.8), the turn relation for this connection can be calculated:

$$\frac{N_3}{N_2 + N_3} = \frac{V_Q}{V_{ax}} = \frac{\sin(30° - |\delta|)}{\sin(30° + |\delta|)} \tag{A.9}$$

$$\frac{N_1}{N_2 + N_3} = \frac{1}{2\sin(30° + |\delta|)} \frac{V_{AB}}{V_{ab}} \tag{A.10}$$

For this connection the angle between V_{ab} and V_{AB}, δ, is negative, as V_{ab} lags V_{AB}, and it is in a range of -30º to 0º. Seeing the extreme cases, if δ = -30º the secondary winding will

remain as coils N_2 in reverse delta connection. If δ = 0º, the secondary winding will be in wye connection.

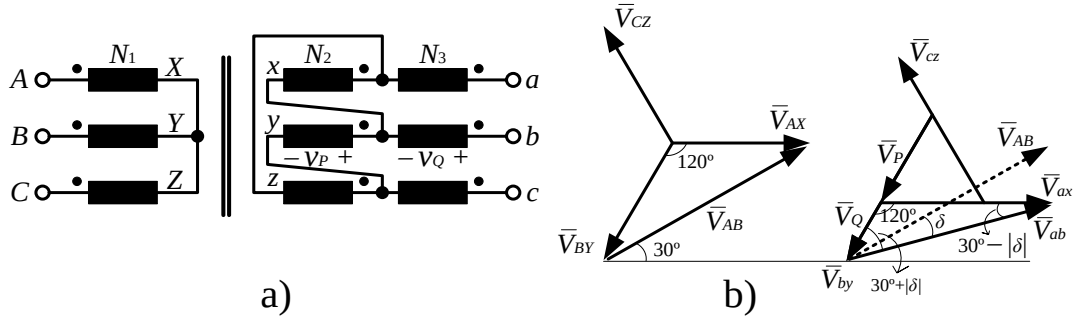


Figure A.5. Representation of connection Y/Z-2 a), and its phasors diagram b).

A.2.3.2. Connection Δ/Z-1

Connection Δ/Z-1 is illustrated in Figure A.6.a). In this case, the primary winding is delta-connected and the secondary has the same Z-1 connection explained in subsection A.2.2.

From phasors diagram in Figure A.6.b), and the trigonometrical process previously explained, the turns ratios can be deduced:

$$\frac{N_3}{N_2+N_3}=\frac{V_Q}{V_{ax}}=\frac{\sin(|\delta|)}{\sin(60°-|\delta|)} \tag{A.11}$$

$$\frac{N_1}{N_2+N_3}=\frac{\sqrt{3}}{2\sin(60°-|\delta|)}\frac{V_{AB}}{V_{ab}} \tag{A.12}$$

As in the previous case, this connection achieves a negative angle between V_{ab} and V_{AB}, that is also in the range of -30º to 0º. The extreme cases would be the secondary winding delta-connected if δ = 0º, or wye-connected if δ = -30º.

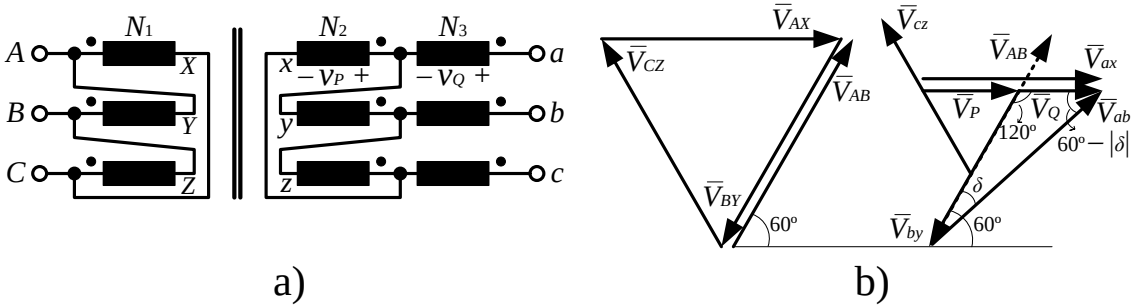


Figure A.6. Illustration of connection Δ/Z-1 a), and its phasors diagram b).

A.2.3.3. Connection Δ/Z-2

Connection Δ/Z-2 is similar to connection Δ/Z-1, but with the secondary coils N_2 delta-connected in reverse order (see Figure A.7.a)). Analyzing the phasors diagram of Figure A.7.b) the relationship for the transformer coils can be achieved:

$$\frac{N_3}{N_2 + N_3} = \frac{V_Q}{V_{ax}} = \frac{\sin(60° - |\delta|)}{\sin(|\delta|)} \tag{A.13}$$

$$\frac{N_1}{N_2 + N_3} = \frac{\sqrt{3}}{2\sin(|\delta|)} \frac{V_{AB}}{V_{ab}} \tag{A.14}$$

In this connection the negative angle, δ, ranges from -60º to -30º. Analyzing the extreme cases the reader can see that if δ = -30º the secondary winding is wye-connected, and if δ = -60º, this winding is inverse delta-connected.

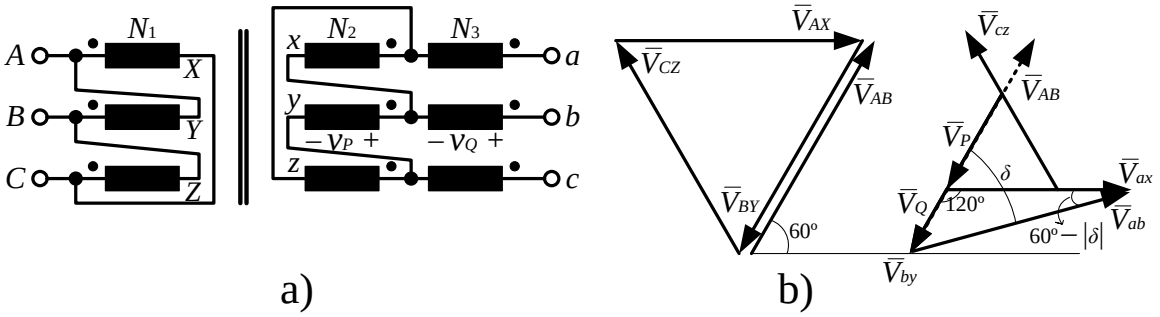


Figure A.7. Representation of connection Δ/Z-2 a), and its phasors diagram b).

A.3. Multi-pulse transformers

The term multi-pulse is often used to refer those power converters that operate in three-phase systems and provide more than six DC-pulses per cycle, in fact, they provide a multiple of six pulses: 12, 18, …

In a similar sense, a multi-pulse transformer is a multi-winding transformer with one winding in the primary side and more than one windings in the secondary side, with the peculiarity that the secondary windings are phase-shifted from its adjacent an equal angle. The angle between the adjacent windings is calculated dividing 60º into the total number of windings in the secondary side (W):

$$\delta_{adj} = \frac{60°}{W} \tag{A.15}$$

In this way, the secondary windings in a multi-pulse transformer that has two secondary windings will be shifted 30º, the shifting angle will be 20º if there are three secondary windings, 15º of shifting if there are four windings, etc.

Figure A.8 shows an example of multi-pulse transformer with three windings in the secondary side. In that example the primary winding is wye-connected and, as there are three secondary windings, the shifting angle between them must be 20º. So the secondary windings are connected in the following way: Z-2 to achieve δ = -20º, Y to have δ = 0º, and Z-1 to get δ = 20º. An alternative connection for a transformer with three secondary windings would be, for example, connecting the primary winding in delta-connection, and the three secondary windings in delta (δ = 0º), Z-1 (δ = -20º), and Z-2 (δ = -40º). Table A.1 contains some examples of multi-winding connections.

Table A.1. Examples of multi-pulse Transformers connections.

Number of secondary windings	Primary winding connection	Secondary winding connection
2	Y	Y (δ = 0º)
		Δ (δ = 30º)
	Δ	Δ (δ = 0º)
		Y (δ = -30º)
3	Y	Z-2 (δ = -20º)
		Y (δ = 0º)
		Z-1 (δ = 20º)
	Δ	Δ (δ = 0º)
		Z-1 (δ = -20º)
		Z-2 (δ = -40º)
4	Y	Z-2 (δ = -15º)
		Y (δ = 0º)
		Z-1 (δ = 15º)
		Δ (δ = 30º)
	Δ	Δ (δ = 0º)
		Z-1 (δ = -15º)
		Y (δ = -30º)
		Z-2 (δ = -45º)
5	Y	Z-2 (δ = -24º)
		Z-2 (δ = -12º)
		Y (δ = 0º)
		Z-1 (δ = 12º)
		Z-1 (δ = 24º)
	Δ	Δ (δ = 0º)
		Z-1 (δ = -12º)
		Z-1 (δ = -24º)
		Z-2 (δ = -36º)
		Z-2 (δ = -48º)

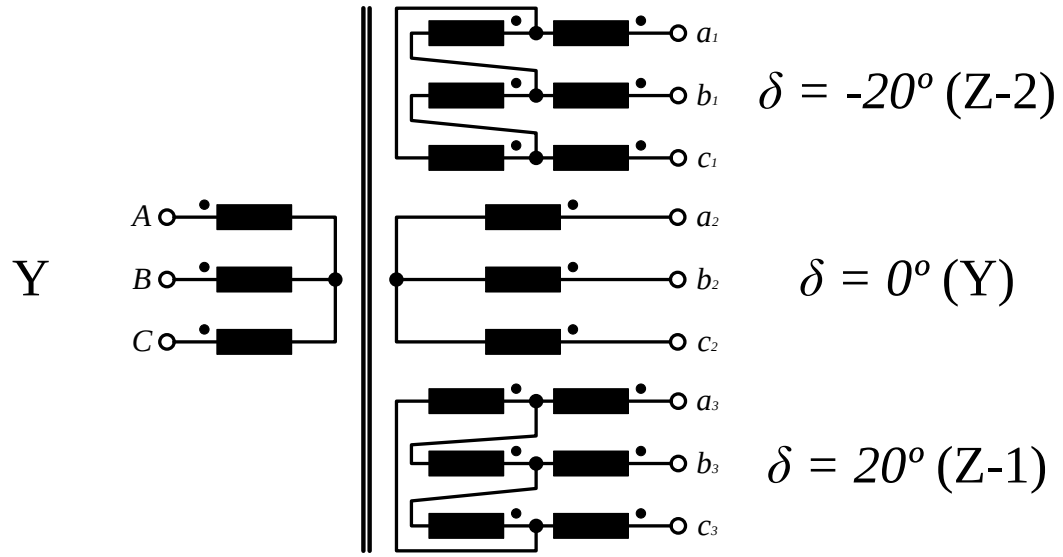


Figure A.8. Example of multi-pulse transformer with three windings in the secondary side.

The objective of having multiple secondary windings with specific shift angle between them is to achieve a phase displacement in the harmonic currents in order to cancel some of them generated by three-phase non-linear loads.

With the purpose of studying how certain harmonics are cancelled using multi-pulse transformers, the current harmonics of a delta/wye transformer connected to a non-linear load and fed by a balanced three-phase voltage source will be analyzed (see Figure A.9). As was mentioned earlier, transformer in Figure A.9 has a phase angle of δ = -30º, and in this case the turns relationship is $N_1 / N_2 = \sqrt{3}$.

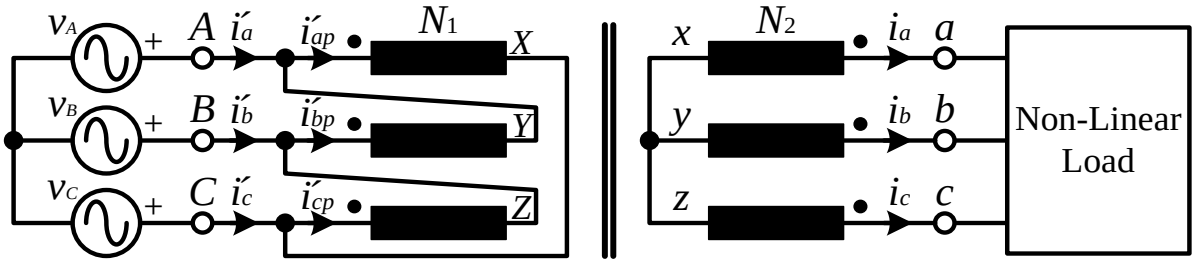


Figure A.9. Delta/wye transformer fed by a balanced source and connected to a non-linear load.

Considering that this is a balanced system, the currents in the non-linear load will be the following:

$$i_a = \sum_{n=1,5,7,11,\ldots}^{\infty} \hat{I}_n \, sin(n\omega t) \tag{A.16}$$

$$i_b = \sum_{n=1,5,7,11,\ldots}^{\infty} \hat{I}_n \sin\big(n(\omega t - 120°)\big)$$

$$i_c = \sum_{n=1,5,7,11,\ldots}^{\infty} \hat{I}_n \sin\big(n(\omega t - 240°)\big)$$

$\hat{I}_n$ in equation (A.16) represents the amplitude of the n^{th} harmonic current. The currents in (A.16) can be referred to the primary winding using the turns relationship:

$$\begin{aligned} i'_{ap} &= i_a \frac{N_2}{N_1} = \frac{1}{\sqrt{3}}\big(\hat{I}_1 \sin(\omega t) + \hat{I}_5 \sin(5\omega t) + \hat{I}_7 \sin(7\omega t) + \hat{I}_{11} \sin(11\omega t) + \cdots\big) \\ i'_{bp} &= i_b \frac{N_2}{N_1} = \frac{1}{\sqrt{3}}\big(\hat{I}_1 \sin(\omega t - 120°) + \hat{I}_5 \sin(5\omega t - 240°) + \hat{I}_7 \sin(7\omega t - 120°) \\ &\quad + \hat{I}_{11} \sin(11\omega t - 240°) + \cdots\big) \\ i'_{cp} &= i_c \frac{N_2}{N_1} = \frac{1}{\sqrt{3}}\big(\hat{I}_1 \sin(\omega t - 240°) + \hat{I}_5 \sin(5\omega t - 120°) + \hat{I}_7 \sin(7\omega t - 240°) \\ &\quad + \hat{I}_{11} \sin(11\omega t - 120°) + \cdots\big) \end{aligned} \tag{A.17}$$

From (A.17) the currents in the primary side, i'_a, i'_b, and i'_c can be obtained:

$$\begin{aligned} i'_a &= i'_{ap} - i'_{bp} = \hat{I}_1 \sin(\omega t + 30°) + \hat{I}_5 \sin(5\omega t - 30°) + \hat{I}_7 \sin(7\omega t + 30°) \\ &\quad + \hat{I}_{11} \sin(11\omega t - 30°) + \cdots \\ i'_b &= i'_{bp} - i'_{cp} = \hat{I}_1 \sin(\omega t - 90°) + \hat{I}_5 \sin(5\omega t + 90°) + \hat{I}_7 \sin(7\omega t - 90°) \\ &\quad + \hat{I}_{11} \sin(11\omega t + 90°) + \cdots \\ i'_c &= i'_{cp} - i'_{ap} = \hat{I}_1 \sin(\omega t - 210°) + \hat{I}_5 \sin(5\omega t + 210°) + \hat{I}_7 \sin(7\omega t - 210°) \\ &\quad + \hat{I}_{11} \sin(11\omega t + 210°) + \cdots \end{aligned} \tag{A.18}$$

Generalizing for any phase and any δ:

$$i'_x = \sum_{n=1,7,13,\ldots}^{\infty} \hat{I}_n \sin\big(n\omega t - (\delta - \varphi_x)\big) + \sum_{n=5,11,17,\ldots}^{\infty} \hat{I}_n \sin\big(n\omega t + (\delta - \varphi_x)\big) \tag{A.19}$$

Where x represents phase A, B or C, φ_x is the angle of each phase (0º, -120º, and -240º for A, B and C respectively in a balanced system). The first $\sum$ in equation (A.19) represents the harmonic currents with positive sequence (n = 1, 7, 13, …), and the second one represents the negative sequence harmonic currents (n = 5, 11, 17, …).

Comparing the line currents in the primary and secondary sides of phase A, for example, (i'_a and i_a), it can be seen that

$$\angle i'_{an} = \angle i_{an} - \delta \qquad \text{for n = 1, 7, 13, 19, … (positive sequence harmonics)} \tag{A.20}$$

$\angle i'_{an} = \angle i_{an} + \delta$ for n = 5, 11, 17, 23, … (negative sequence harmonics)

The relationship between the phase angles of the secondary harmonic currents referred to the primary in a phase shifting transformer is described in (A.20). It can be proved that this equation is valid for any value of δ.

Having in mind expression (A.20), let's analyze the currents in the multi-pulse transformer shown in Figure A.10. All the secondary windings in the multi-pulse transformer shown in Figure A.10 have the same turns ratio: $V_{AB}/V_{ab1} = V_{AB}/V_{ab2} = V_{AB}/V_{ab3} = V_{AB}/V_{ab4} = 4$.

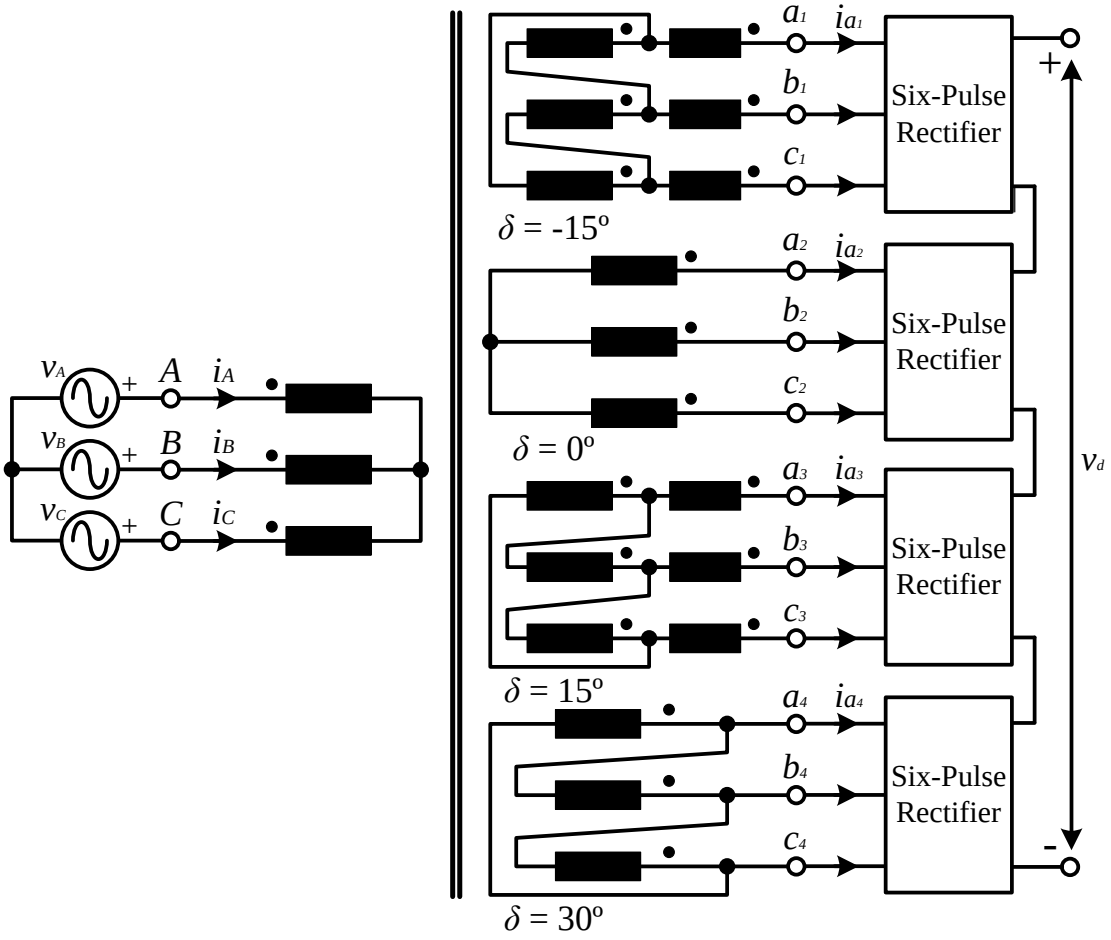


Figure A.10. Example of 24-pulse rectifier to illustrate the harmonic cancellation.

With these conditions, the line currents in the secondary windings are described with the following equations:

$$i_{a_1} = \sum_{n=1,5,7,11,13,\ldots}^{\infty} \hat{I}_n \sin(n\omega t - 15°) \qquad \text{(A.21)}$$

$$i_{a_2} = \sum_{n=1,5,7,11,13,\dots}^{\infty} \hat{I}_n \sin(n\omega t)$$

$$i_{a_3} = \sum_{n=1,5,7,11,13,\dots}^{\infty} \hat{I}_n \sin(n\omega t + 15°)$$

$$i_{a_4} = \sum_{n=1,5,7,11,13,\dots}^{\infty} \hat{I}_n \sin(n\omega t + 30°)$$

As the reader can suppose, the primary current can be calculated as the sum of the secondary currents referred to the primary:

$$i_A = i'_{a_1} + i'_{a_2} + i'_{a_3} + i'_{a_4} \tag{A.22}$$

The secondary currents referred to the primary can be obtained from (A.19):

$$i'_{a_1} = \frac{1}{4}\left(\sum_{n=1,7,13,\dots}^{\infty} \hat{I}_n \sin(n(\omega t - 15°) + 15°) + \sum_{n=1,7,13,\dots}^{\infty} \hat{I}_n \sin(n(\omega t - 15°) - 15°) \right)$$

$$\begin{aligned} i'_{a_1} = \frac{1}{4}\big(& \hat{I}_1 \sin(\omega t) + \hat{I}_5 \sin(5\omega t - 90°) + \hat{I}_7 \sin(7\omega t - 90°) + \hat{I}_{11} \sin(11\omega t - 180°) \\ & + \hat{I}_{13} \sin(13\omega t - 180°) \\ & + \hat{I}_{17} \sin(17\omega t - 270°) + \hat{I}_{19} \sin(19\omega t - 270°) + \hat{I}_{23} \sin(23\omega t) + \cdots \big) \end{aligned} \tag{A.23}$$

$$\begin{aligned} i'_{a_2} = \frac{1}{4}\big(& \hat{I}_1 \sin(\omega t) + \hat{I}_5 \sin(5\omega t) + \hat{I}_7 \sin(7\omega t) + \hat{I}_{11} \sin(11\omega t) \\ & + \hat{I}_{13} \sin(13\omega t) + \hat{I}_{17} \sin(17\omega t) + \hat{I}_{19} \sin(19\omega t) + \hat{I}_{23} \sin(23\omega t) \\ & + \cdots \big) \end{aligned} \tag{A.24}$$

$$i'_{a_3} = \frac{1}{4}\left(\sum_{n=1,7,13,\dots}^{\infty} \hat{I}_n \sin(n(\omega t + 15°) - 15°) + \sum_{n=1,7,13,\dots}^{\infty} \hat{I}_n \sin(n(\omega t + 15°) + 15°) \right)$$

$$\begin{aligned} i'_{a_3} = \frac{1}{4}\big(& \hat{I}_1 \sin(\omega t) + \hat{I}_5 \sin(5\omega t + 90°) + \hat{I}_7 \sin(7\omega t + 90°) + \hat{I}_{11} \sin(11\omega t + 180°) \\ & + \hat{I}_{13} \sin(13\omega t + 180°) \\ & + \hat{I}_{17} \sin(17\omega t + 270°) + \hat{I}_{19} \sin(19\omega t + 270°) + \hat{I}_{23} \sin(23\omega t) + \cdots \big) \end{aligned} \tag{A.25}$$

$$i'_{a_4} = \frac{1}{4}\left(\sum_{n=1,7,13,\dots}^{\infty} \hat{I}_n \sin(n(\omega t + 30°) - 30°) + \sum_{n=1,7,13,\dots}^{\infty} \hat{I}_n \sin(n(\omega t + 30°) + 30°) \right)$$

$$\begin{aligned} i'_{a_4} = \frac{1}{4}\big(& \hat{I}_1 \sin(\omega t) + \hat{I}_5 \sin(5\omega t + 180°) + \hat{I}_7 \sin(7\omega t + 180°) + \hat{I}_{11} \sin(11\omega t) \\ & + \hat{I}_{13} \sin(13\omega t) + \hat{I}_{17} \sin(17\omega t + 180°) + \hat{I}_{19} \sin(19\omega t + 180°) \\ & + \hat{I}_{23} \sin(23\omega t) + \cdots \big) \end{aligned} \tag{A.26}$$

So, from equations (A.22) to (A.26) the reader can find that:

$$i_A = \hat{I}_1\, sin(\omega t) + \hat{I}_{23}\, sin(23\omega t) + \hat{I}_{25}\, sin(25\omega t) + \hat{I}_{47}\, sin(47\omega t) + \cdots \quad \text{(A.27)}$$

As it can be seen in (A.27), using the multi-pulse transformer shown in Figure A.10, the primary current only contains the following harmonics, apart from the fundamental one:

$$n = k(4 \cdot 6) \pm 1 \qquad \text{for } k = 1, 2, 3, \ldots \quad \text{(A.28)}$$

The previous equation describes the situation for a multi-pulse transformer with four secondary windings. In the case of having a transformer with *W* secondary windings where the angle between adjacent winding is calculated as in (A.15), the primary current would be described as:

$$i_A = \hat{I}_1\, sin(\omega t) + \sum_{k=1,2,3,\ldots}^{\infty} \hat{I}_{(6kW-1)}\, sin\big((6kW-1)\omega t\big) + \hat{I}_{(6kW+1)}\, sin\big((6kW+1)\omega t\big) \quad \text{(A.29)}$$

Appendix B: POWER QUALITY APPLICATIONS. STATCOM DESCRIPTION AND CONTROL

A STATtic COMpensator (STATCOM) is an application widely used in medium voltage systems because it can produce or consume reactive power depending on the system requirements. In other words, a STATCOM can behave as a reactive power source or sink.

B.1. STATCOM system description

A STATtic COMpensator is an application widely used in medium voltage systems because it can produce or consume reactive power depending on the system requirements. In other words, a STATCOM can behave as a reactive power source or sink.

A STATCOM is basically composed of a voltage source converter (VSC) connected to the grid through an inductive filter and the control loops and algorithms needed to control it. The point where the STATCOM is connected to the grid is known as point of common coupling (PCC). An example of a control system for a STATCOM could be as the diagram shown in Figure B.1.

The shaded part in Figure B.1 represents the control part of the STATCOM system. This control system consists on some SISO controllers cascaded connected: with two inner control loops and two outer loops. The inner controllers are for the two current components (i_d and i_q) and they must be at least ten times faster than the outer controllers, which are for the active and reactive power respectively. Maintaining this time constraint allows tuning the outer controllers without having into account the inner controllers' dynamics. This fact makes easier the controllers' tuning, but it has a disadvantage: the sample period can be at most about

200 μs, in order to allow the settling time of the complete control loop be around hundreds of milliseconds.

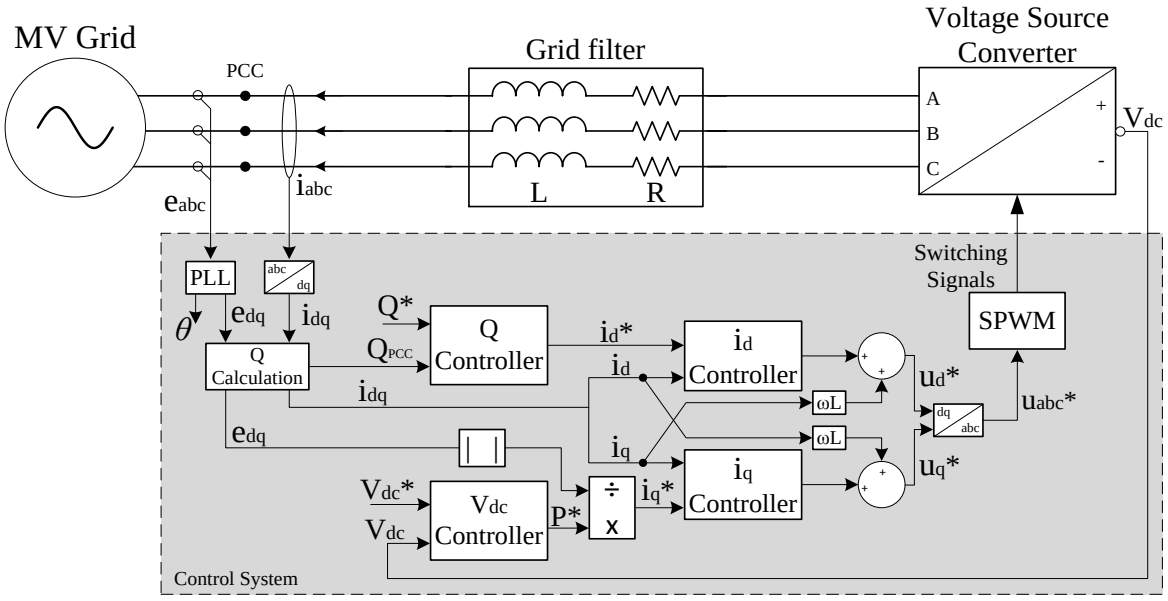


Figure B.1. STATCOM control system diagram

The main characteristics of the STATCOM system shown in Figure B.1 are summarized as follows:

– All the transformations between *abc* ↔ *dq* components are power invariant. The equations needed to do this transformation are shown in (B.1) and (B.2), being *S* the transformed variable in each case:

$$\vec{S}_{dq0} = T_{abc\to dq0} \cdot \vec{S}_{abc} = \begin{bmatrix} S_d(t) \\ S_q(t) \\ S_0(t) \end{bmatrix} = \sqrt{\frac{2}{3}} \cdot \begin{bmatrix} \cos\theta & \sin(\theta - \frac{\pi}{6}) & -\sin(\theta + \frac{\pi}{6}) \\ -\sin\theta & \sin(\theta + \frac{\pi}{3}) & \sin(\theta - \frac{\pi}{3}) \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \cdot \begin{bmatrix} S_a(t) \\ S_b(t) \\ S_c(t) \end{bmatrix} \quad \text{(B.1)}$$

$$\vec{S}_{abc} = T_{dq0\to abc} \cdot \vec{S}_{dq0} = \begin{bmatrix} S_a(t) \\ S_b(t) \\ S_c(t) \end{bmatrix} = \sqrt{\frac{2}{3}} \cdot \begin{bmatrix} \cos\theta & -\sin\theta & 1/\sqrt{2} \\ \sin(\theta - \frac{\pi}{6}) & \sin(\theta + \frac{\pi}{3}) & 1/\sqrt{2} \\ -\sin(\theta + \frac{\pi}{6}) & \sin(\theta - \frac{\pi}{3}) & 1/\sqrt{2} \end{bmatrix} \cdot \begin{bmatrix} S_d(t) \\ S_q(t) \\ S_0(t) \end{bmatrix} \quad \text{(B.2)}$$

– The PLL (Phase Locked Loop) monitors and synchronizes the converter with the grid, providing the information of the PCC voltage, the frequency and the phase to the control system. The PLL is programmed such that the grid voltage vector is located in the q-axis, what means

$$\begin{cases} e_{dPCC} = 0 \\ e_{qPCC} = |\vec{e}_{PCC}| \end{cases} \quad \text{(B.3)}$$

And this also means that (ideally)

$$\begin{cases} P_{PCC} = e_{qPCC} \cdot i_q \\ Q_{PCC} = e_{qPCC} \cdot i_d \end{cases} \quad \text{(B.4)}$$

This is the same to say that active power depends on the q-component of the current, and reactive power depends on d-component. This fact allows to have decoupled controllers for active and reactive power.

The equations shown in (B.4) describe an ideal situation. In order to contemplate non-ideal situations in the described system the implemented equations will be the following:

$$\begin{cases} P_{PCC} = e_{dPCC} \cdot i_d + e_{qPCC} \cdot i_q \\ Q_{PCC} = -e_{dPCC} \cdot i_q + e_{qPCC} \cdot i_d \end{cases} \quad \text{(B.5)}$$

There are four controllers that have all a similar structure: proportional-integral (PI) controllers with anti-windup. The inner controllers are the *dq*-current controllers, and the outer controllers are for the active and the reactive power. To controlling the active power, it will be used the converter DC voltage, as almost all the active power will be consumed in order to maintain the desired voltage in the converter capacitor or capacitors. The reactive power is controlled in such way that the displacement power factor (DPF) is as close to 1 as possible. Table B.1 summarizes the main parameters of the mentioned controllers, being T_S the system sample time, ζ the damping ratio of the controllers, and t_{s_xx} the settling time for each controller.

Table B.1. Main parameters of the controllers in the STATCOM system.

	Inputs	**Outputs**	**Control parameters**
Current controllers	References: i_d^*, i_q^* Controlled signals: i_d, i_q	Output signals: v_d^*, v_q^*	$\zeta = 0.707$ $ts\_id = ts\_iq \geq 10\ T_S$
V_{dc} controller	Reference: V_{dc}^* Controlled signal: V_{dc}	Output signal: i_q^*	$\zeta = 0.707$ $ts\_dc \geq 10\ ts\_iq$
Q controller	Reference: Q^* Controlled signal: Q	Output signal: i_d^*	$\zeta = 0.707$ $ts\_Q \geq 10\ ts\_id$

B.1.2. Current controllers

For this STATCOM system the chosen grid filter is type L (in Figure B.1 also the associated resistance *R* is represented), so the current controllers have been designed having into account the value of this inductance (*L*).

The plant identification process for the current controllers is done assuming that the voltage source converter's behavior is ideal. That means that the converter output voltages $u_a(t)$, $u_b(t)$, and $u_c(t)$ are sinusoidal, and their vector representation is the same as the reference that is applied to the PWM generator, $\vec{u}^*(t)$. In these conditions the plant is described in the continuous space and in *dq*-axis as:

$$\vec{u}^*(t) = R\,\vec{i}_g(t) + L\,\frac{d\vec{i}_g(t)}{dt} + j\omega L\vec{i}_g(t) + \vec{e}_g(t) \tag{B.6}$$

where $\vec{u}^*(t)$ is the vector that represents the voltage references for the PWM generator, *L* is the value of the filter inductance, *R* is the associated resistance of the filter inductance, $\vec{i}_g(t)$ is grid currents vector, $\vec{e}_g(t)$ is the grid voltages vector, and ω is the speed of vector $\vec{e}_g(t)$ that is measured by the PLL block in Figure B.1 ($\theta = \int_0^t \omega\, dt$).

The vector transfer function of the plant in the *s*-plane using *dq*-axis and considering $\vec{e}_g(t)$ as a perturbation is the following:

$$\vec{T}(s) = \frac{\vec{i}_g}{\vec{u}} = \frac{1}{R + sL + j\omega L} \tag{B.7}$$

The first step in the controllers design consists on cancelling the crossing coupling between the *dq*-currents due to the term '$j\omega L$' in equation (B.7). In order to achieve this objective, in this case a negative feedback loop with gain value of '$-j\omega\hat{L}$' is added as shown in Figure B.2. The result is a new transfer function $\vec{T}'(s)$:

$$\vec{T}'(s) = \frac{\vec{i}_g}{\vec{u}'} = \frac{\vec{T}(s)}{1 - \vec{T}(s)j\omega\hat{L}} = \frac{\dfrac{1}{R + sL + j\omega L}}{1 - \dfrac{j\omega\hat{L}}{R + sL + j\omega L}} = \frac{1}{R + sL + j\omega(L - \hat{L})} \tag{B.8}$$

If $L - \hat{L} = 0$ then $\vec{T}'(s)$ is

$$\vec{T}'(s) = \frac{\vec{i}_g}{\vec{u}'} = \frac{1}{R + sL} \tag{B.9}$$

Variables with ^ represent nominal or measured values of the components before the converter startup. During the converter operation these values can vary. So, variables with the

symbol ^ are used in the controller design, and without this symbol the variables represent the plant elements.

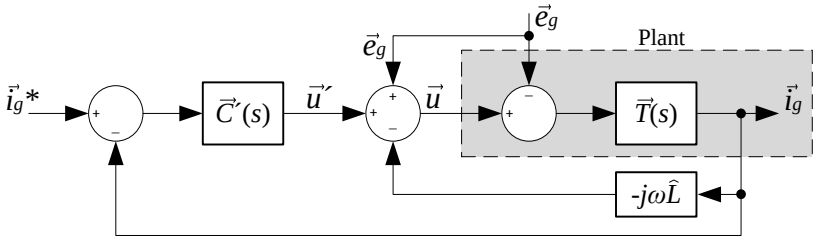


Figure B.2. Current controller vector scheme with decoupling between dq-components and feedforward compensation of $\vec{e}_g$.

The second step consists on cancelling the grid voltage ($\vec{e}_g(t)$) effect through a feedforward compensation as shown in Figure B.2. This is possible because the $\vec{e}_g(t)$ dynamics is much slower than the grid current dynamics and so, $\vec{e}_g(t)$ can be considered as a system perturbation. This feedforward compensation also allows (ideally) compensate any perturbation happened in the power grid and therefore it improves the system dynamics. In this way, the controller's equation in the time domain is:

$$\vec{u}(t) = \vec{u}'(t) + j\omega\hat{L}\vec{i}_g(t) + \vec{e}_g(t) \tag{B.10}$$

where $\vec{u}'(t)$ is the output of the controller $\vec{C}'(s)$, $j\omega\hat{L}\vec{i}_g(t)$ is the decoupling current components term, and $\vec{e}_g(t)$ is the feedforward term.

Figure B.3 represents the same controller vector diagram as Figure B.2 but in scalar *dq*-components. If $L - \hat{L} = 0$ the feedforward compensation is ideal and the current controller is the shown in Figure B.4, where there is not coupling between the current components and the grid voltage disappears from the system dynamics. As it can be seen in Figure B.4, the close-loop analysis is the same for *d*-axis and *q*-axis, so it is enough to study one of them to obtain the transfer functions $\vec{C}'_d(s)$ and $\vec{C}'_q(s)$. In this way, the vector transfer function shown in equation (B.9), $\vec{T}'(s)$, has been changed in a scalar first order transfer function:

$$T'(s) = \frac{i_g}{u'} = \frac{1}{R + sL} \tag{B.11}$$

The next step in the controller designing process consists on discretizing the plant model $T'(s)$ shown in (B.11). Although $u'(s)$ is PWM signal, here it is supposed to be a sinewave signal in order to consider that it is constant in a sample period. Doing this assumption and applying the Zero Order Hold (ZOH) discretization method the discrete plant is obtained:

$$T'(z) = (1 - z^{-1})Z\left[\frac{T'(s)}{s}\right] = \frac{\frac{1}{R}\left(1 - e^{-R\,T_S/L}\right)z^{-1}}{1 - e^{-R\,T_S/L}\,z^{-1}} = \frac{bz^{-1}}{1 - az^{-1}} = \frac{b}{z - a} \tag{B.12}$$

According with the above, the obtained current controller block diagram is the shown in Figure B.5. In this diagram an anti-windup has been added.

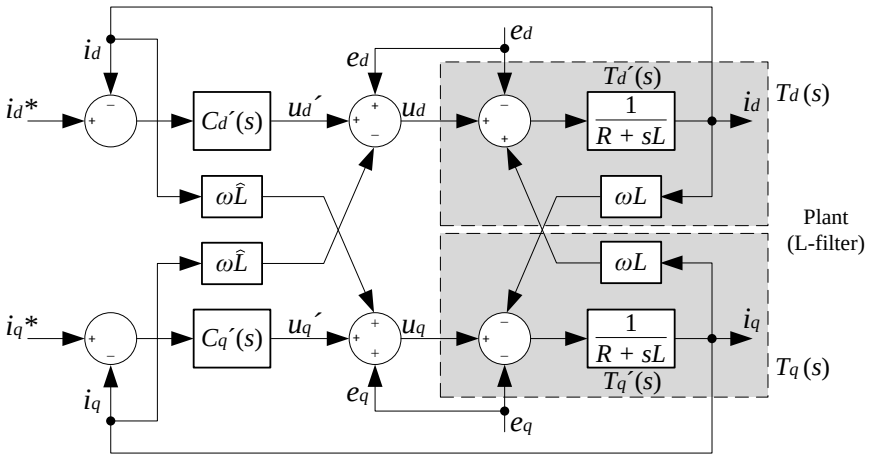


Figure B.3. Current controllers in dq-components block diagram.

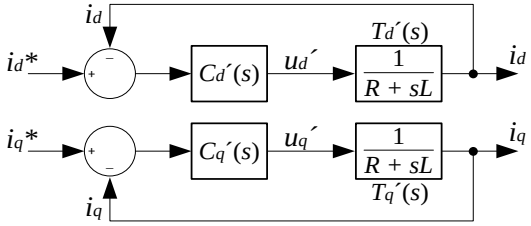


Figure B.4. Scheme of current controllers with ideal decupling of dq-components and feedforward compensation.

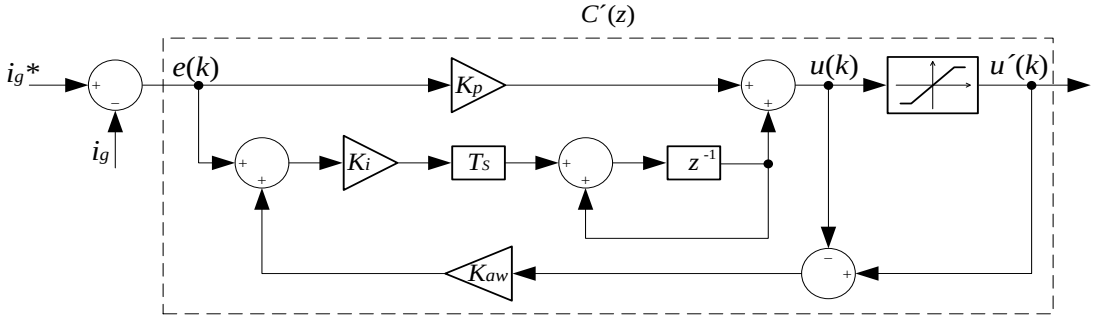


Figure B.5. Current controller for the STATCOM system.

To assume that the plant follows the equation (B.12), what is the same to say that the computational delay is not taken into account, the controller settling time (t_s) should be

defined between five and ten times higher than the sample time (T_S). Besides to the diagram shown in Figure B.5 the feedforward and the crossing decoupling should be added, so the input voltage for the PWM generator is:

$$\vec{u}(k) = \vec{u}'(k) + j\omega L \frac{\vec{i}_g{}^*(k) + \vec{i}_g(k)}{2} + \vec{e}_g(k) \tag{B.13}$$

And the controller has the following expression:

$$C'(z) = k_p + k_i \frac{T_S}{z-1} = k_p \frac{z-\alpha}{z-1} \tag{B.14}$$

In this way, the loop gain $T'(z) \cdot C'(z)$ has two poles located in $p_1 = 1$, and $p_2 = a$ very close to 1, and a zero located in $z = \alpha$, as shown in Figure B.6. Depending on the controller gain, the close-loop system may also have two complex conjugate poles. In this case the general formula for the close-loop transfer function denominator is

$$D(z) = (z - \rho e^{j\vartheta})(z - \rho e^{-j\vartheta}) = z^2 - (2\rho\cos\vartheta)z + \rho^2 \tag{B.15}$$

where $\rho = e^{-(\zeta\omega_n T_S)}$, and $\vartheta = \omega_n T_S\sqrt{1-\zeta^2}$. So, it implies that:

$$k_p = \frac{1 + a - 2\rho\cos\vartheta}{b}; \qquad \alpha = \frac{a - \rho^2}{1 + a - 2\rho\cos\vartheta}; \qquad k_i = \frac{k_p}{T_S}(1-\alpha) \tag{B.16}$$

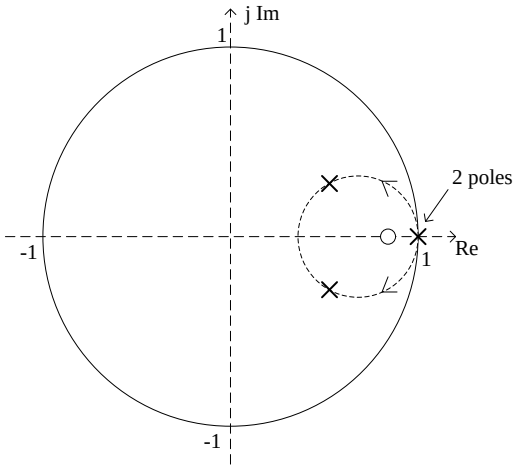


Figure B.6. Root locus for the close-loop function $T'(z) \cdot C'(z)$.

In this case, as the used sample time is T_s = 100 μs, the chosen value for the settling time is t_{sC} = 7.5 ms. The damping ratio is ζ = 0.707, and the relationship between t_s and ω_n is

$$t_s \approx \frac{4.6}{\zeta \cdot \omega_n} \tag{B.17}$$

Finally, the value for the anti-windup gain is usually chosen as the inverse of the proportional gain, $k_{aw} = {}^{1}/_{k_p}$.

B.1.3. Active power controller

In the described STATCOM system the control of the active power is done through a DC-bus voltage controller. This is because in this kind of application there are not elements that generate power, there are only capacitors, and the active power exchanged is very low (only the converter losses). So, the DC-bus controller duty is to maintain constant the DC-bus voltage. The DC-bus controller, which indirectly controls the active power, sends the active current reference to the current controller.

As in the previous controller design, the first step is identifying the plant. In this case, the DC-bus is modeled as an ideal capacitor. Its dynamic equivalent circuit is represented in Figure B.7. When the STATCOM system is based in a multilevel converter, as it happens in this case, the DC-bus is modeled as the equivalent capacity of all the capacitors that compose the DC-bus.

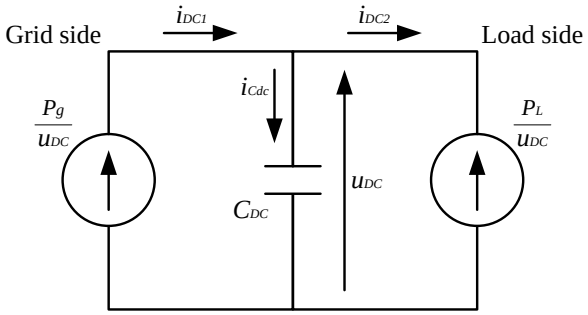


Figure B.7. DC-bus Dynamic equivalent circuit.

In Figure B.7 the following variables appear:

- C_{DC} is the ideal DC-bus capacity.
- u_{DC} is the DC-bus voltage.
- i_{Cdc} is the current through C_{DC}.
- i_{DC1} is the DC-bus current in the grid side.
- i_{DC2} is the DC-bus current in the load side.
- P_g is the grid active power.
- P_L is the load active power.

In this case the DC-bus model will be based in the stored energy in the capacitor. The temporal variation in this energy is calculated as the instant subtraction of the grid and load powers with the signs that are represented in Figure B.7. In this way:

$$\frac{1}{2}C_{DC}\frac{du_{DC}^2}{dt} = P_g - P_L = e_q i_q - P_L \tag{B.18}$$

If we define $W = u_{DC}^2$ [129], the previous equation can be reformulated as a first order system:

$$\frac{1}{2}C_{DC}\frac{dW}{dt} = e_q i_q - P_L \tag{B.19}$$

Linearizing equation (B.19) through a small-signal modelling, despising the second order perturbations and considering that in steady state $e_q i_q = P_L$, the following equation is obtained:

$$\frac{1}{2}C_{DC}\frac{d\widetilde{W}}{dt} = e_q \tilde{\imath}_q + \tilde{e}_q i_q - \tilde{P}_L \tag{B.20}$$

In this case, the transfer function to be searched is $\widetilde{W}/\tilde{\imath}_q$. The perturbations are considered zero but $\tilde{P}_L$ due to it depends on $\widetilde{W}$ and on the DC-bus load. So, equation (B.20) is transformed into

$$\frac{1}{2}C_{DC}\frac{d\widetilde{W}}{dt} = e_q \tilde{\imath}_q - \tilde{P}_L \tag{B.21}$$

From (B.21) and supposing that $\tilde{P}_L = \widetilde{W}/_{R_L}$(being R_L the resistance in the load side), the relationship between $\tilde{\imath}_q$ and $\widetilde{W}$ in the Laplace domain is

$$\frac{\widetilde{W}}{\tilde{\imath}_q}(s) = \frac{e_q R_L}{\frac{C_{DC}R_L}{2}s + 1} \tag{B.22}$$

If satisfied that $C_{DC}R_L \geq 40T_S$, that is very usual, the equation (B.22) can be approximated as

$$\frac{\widetilde{W}}{\tilde{\imath}_q}(s) = \frac{2e_q}{sC_{DC}} \tag{B.23}$$

In this way the controller constants' values are independent from R_L. Additionally, the previous equation can be made independent from the grid voltage (that may have variations) with the following transformation:

$$\frac{\widetilde{W}}{\widetilde{P}_g}(s) = \frac{2}{sC_{DC}} \tag{B.24}$$

So, the plant model used in this case will be the expressed in the transfer function (B.24). Figure B.8 represents this transfer function considering $\widetilde{P}_g$ as a system perturbation, and it can be expressed as

$$G(s) = \frac{2}{sC_{DC}} \tag{B.25}$$

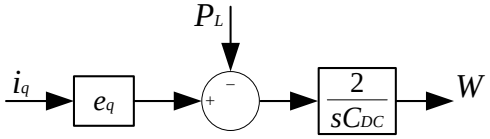


Figure B.8. Approximate model of the DC-bus independent of the R_L.

Figure B.9 represents the control loop of u_{DC}. In that figure a ZOH block has been added as the control proposals are in discrete domain. Previously to the ZOH block the current controller has been included. In this way, the transfer function of the proportional-integral (PI) controller is:

$$\frac{P_g^*}{u_{DC}^{2\,*} - u_{DC}^2} = k_{pDC}\frac{z - \alpha_{DC}}{z - 1} \tag{B.26}$$

being k_{pDC} and α_{DC} the constants of the DC-bus voltage PI controller. If the u_{DC} controller and the current controller are perfectly decoupled the block diagram can be simplified as shown in Figure B.10. To consider both controllers decoupled the DC- bus controller settling time must be at least ten times higher than the settling time for the current controller, in this case t_{sDC} = 100 ms. Besides that, in order to avoid high overvoltage in u_{DC}, the damping ratio should be $\zeta \geq 1/\sqrt{2}$. Under these conditions, and using the same method as in the previous subsection, the constants k_{pDC} and α_{DC} are obtained.

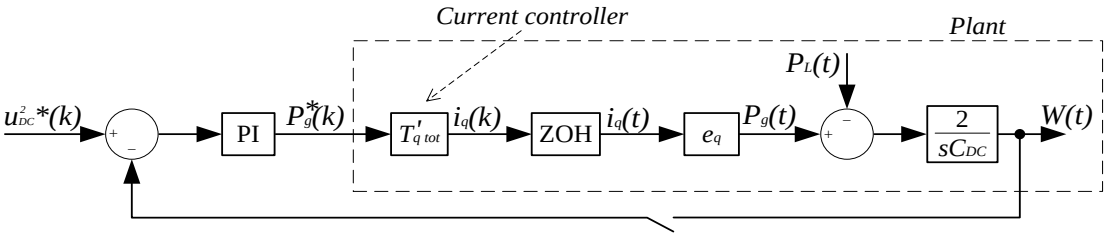


Figure B.9. Control loop of u_{DC} in z-domain considering the capacitor energy as control variable.

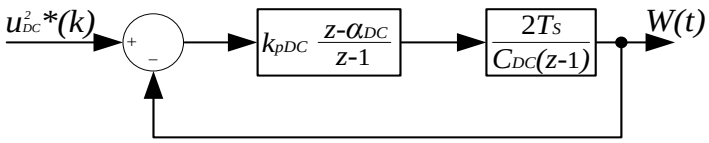


Figure B.10. DC-bus controller considering the voltage and current controllers perfectly decoupled.

Due to an STATCOM exchange reactive power with the grid, the reactive power reference variation implies variations in the fundamental harmonic of the converter output voltage V_{out}, represented in Figure B.11. When the converter works in capacitive mode, the amplitude of V_{out} will take a value higher than the voltage in the PCC, V_{PCC}. Therefore, if the sinusoidal PWM with third harmonic injection is used the following constraint should be fulfilled:

$$\hat{V}_{out}(t) \leq \frac{u_{DC}}{2} \cdot 1.154 = \frac{u_{DC}}{\sqrt{3}} \tag{B.27}$$

On the other hand, when the converter behaves as inductive mode, the amplitude of V_{out} will be lower than the amplitude of V_{PCC}, so, if u_{DC} is maintained constant, the amplitude modulation index will be reduced considerably, which affects to the harmonic content of the output voltage.

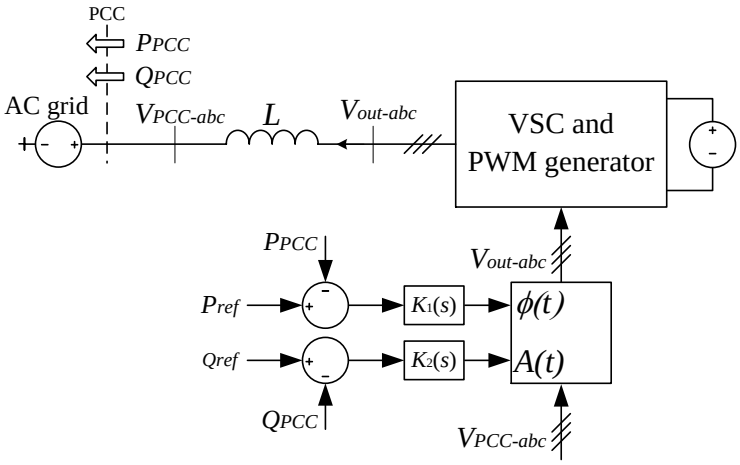


Figure B.11. STATCOM single-line diagram with the used variables for calculate the DC-bus voltage reference.

The objective now is quantify the value of V_{out} in such way that for both, transient and steady states, the value of u_{DC} assures a right operation and the modulation index around 0.9. This makes that the harmonic content of the grid current is almost equal when working in both modes, inductive and capacitive.

So in this case the peak value of V_{out} will be assumed to be the same as in [71]:

$$\hat{V}_{out}(t) = \left\{ \hat{V}_{PCC}^2 + \frac{4}{9}\left(\frac{L\omega}{\hat{V}_{PCC}}\right)^2 (P_{PCC}^2 + Q_{PCC}^2) + \frac{4L\omega}{3} Q_{PCC} + \frac{4}{9}\left(\frac{L\omega}{\hat{V}_{PCC}}\right)^2 \left[\left(\frac{1}{\omega}\frac{dP_{PCC}}{dt}\right)^2 + \left(\frac{1}{\omega}\frac{dQ_{PCC}}{dt}\right)^2\right] + \left[\frac{4L\omega}{3} + \frac{8}{9}\left(\frac{L\omega}{\hat{V}_{PCC}}\right)^2 Q_{PCC}\right]\left(\frac{1}{\omega}\frac{dP_{PCC}}{dt}\right) + \left[-\frac{8}{9}\left(\frac{L\omega}{\hat{V}_{PCC}}\right)^2 P_{PCC}\right]\left(\frac{1}{\omega}\frac{dQ_{PCC}}{dt}\right)\right\}^{\frac{1}{2}} \quad \text{(B.28)}$$

The previous equation is for steady state conditions of active and reactive power (P_{PCC} and Q_{PCC}), and also for transient state conditions ($\frac{dP_{PCC}}{dt}$ and $\frac{dQ_{PCC}}{dt}$).

According to equation (B.27), and in order to determine a value of $\hat{V}_{out}(t)$ than can be software implemented easily, (B.28) is simplified obtaining the following equation:

$$\hat{V}_{out}(t) = \sqrt{\hat{V}_{PCC}^2 + \frac{4}{9}\left(\frac{L\omega}{\hat{V}_{PCC}}\right)^2 \left(P_{PCC}^2 + Q_{PCC}^2\right) + \frac{4L\omega}{3} Q_{PCC}} \approx \sqrt{\hat{V}_{PCC}^2 + \frac{4L\omega}{3} Q_{PCC}} \quad \text{(B.29)}$$

From previous equation, the reference for the DC-bus voltage can be stablished as a function of the reactive power.

Moreover, the most significant transient-state terms can be added to (B.29) to obtain the following equation:

$$\hat{V}_{out}(t) \approx \sqrt{\hat{V}_{PCC}^2 + \frac{4L\omega}{3} Q_{PCC} + \frac{4L}{3}\frac{dP_{PCC}}{dt}} \quad \text{(B.30)}$$

B.1.4. Reactive power controller

The reactive power controller in a STATCOM system may be composed by three different parts that fulfill the following tasks:

- Controlling the reactive power, *Q*.
- Controlling the voltage, *V*.
- Controlling the power factor, PF.

Each one of the previous controllers represents an operation mode of the STATCOM system, and the three of them work over the same parameter in the PCC, what is the same to say that the three modify the reactive power, so also modify the voltage in the point of common coupling, and at the same time they change the power factor. Due to this fact, only one of them can be selected at once.

The three mentioned choices will be explained bellow.

B.1.4.1. Reactive power controller (Q)

Figure B.12 shows the reactive power controller block diagram. With this controller, if the reference Q^* is set to 0, this allows the converter supplies the active power consumed by the grid filter capacitor bank, thus the displacement power factor (DPF) in the PCC will be 1. If this controller is not used the DPF will be lower than 1.

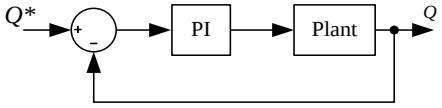


Figure B.12. Reactive power controller (Q-controller).

In Figure B.12 the feedback signal, Q, is obtained through the following equation:

$$Q_{PCC} = -e_{dPCC} \cdot i_q + e_{qPCC} \cdot i_d \tag{B.31}$$

The plant for this controller can be considered to be 1, so the controller's role is to smooth the system response when the reference or the load vary, and to assure that the steady state error is zero.

In order to adjust this controller independently to the inner current control loop, its settling time must be at least ten times slower than the current controller settling time. In this work the chosen value for the settling time is t_{sQ} = 150 ms.

B.1.4.2. Voltage controller (V)

Figure B.13 represents the single-line scheme of a STATCOM system connected to the grid, which Thevenin equivalent circuit is represented by an ideal voltage source and equivalent impedance composed by L_g and R_g.

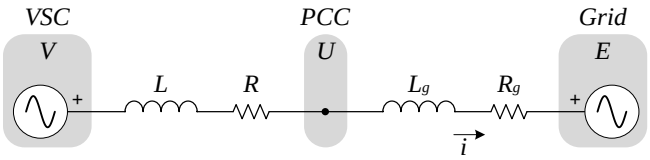


Figure B.13. Single-line scheme of a grid-connected STATCOM system.

From Figure B.13 it is possible to develop the little-signal model in *dq*-components that describes the PCC voltage dynamics:

$$\vec{u}(t) = R_g\vec{i}(t) + L_g\frac{d\vec{i}(t)}{dt} + j\omega\vec{i}(t) + \vec{e}(t) \tag{B.32}$$

If equation (B.32) is decomposed into real and imaginary parts, and assuming that $R_g\vec{i}(t) \approx 0$ and that $L_g \left.\frac{d\vec{i}(t)}{dt}\right/ \approx 0$, due to the PCC voltage control dynamics is very slow, it is obtained the following expressions:

$$\begin{aligned} u_d(t) &= \omega L_g i_q(t) + e_d(t) = 0 \\ u_q(t) &= \omega L_g i_d(t) + e_d(t) \end{aligned} \tag{B.33}$$

u_d = 0 because the PLL that is connected to the PCC is tuned in such way that the projection of the PCC voltage over the *d*-axis is 0, as was mentioned in (B.3). Having those considerations into account, the PCC voltage model can be represented like in Figure B.14.

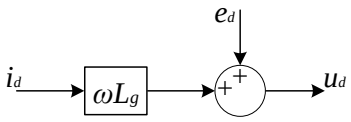


Figure B.14. PCC voltage controller model in dq-axis.

Modifying the PCC voltage is only possible if the grid impedance is not null. In that case, the higher is the grid impedance, the higher will be the range of variation of PCC voltage. If this grid impedance is small, for voltage variations in the PCC it will be essential to inject or consume huge currents into the grid.

The PCC voltage regulation through a STATCOM system is based in the graphic shown in Figure B.15. The different load lines represent the voltage-reactive current characteristic of the grid. Then, if the STATCOM is configured to regulate the PCC voltage, it would be able to set the voltage V_T to the reference voltage independently to the grid load line.

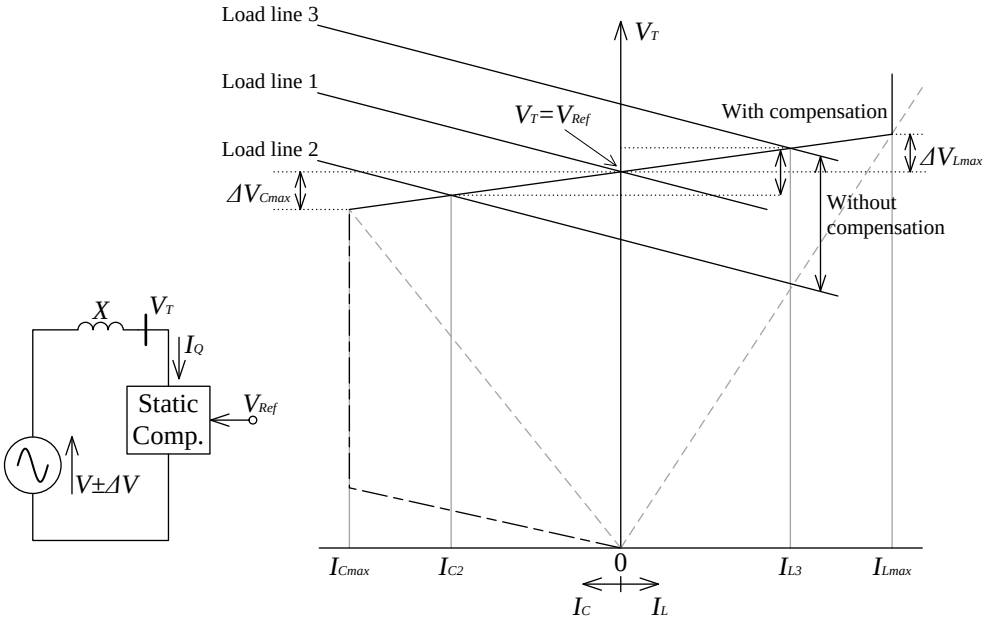


Figure B.15. PCC voltage regulation with a STATCOM system.

The controller proposed in this case is shown in Figure B.16. It consists on a PI controller, an anti-windup gain, and a droop gain that is subtracted from the error between the reference and the measure. The tuning of the controller constants is done as explained in previous subsections.

B.1.4.3. Power factor controller (PF)

The power factor controller consists on using the reactive power controller but giving as reference the following:

$$q^* = \frac{p}{PF^*}\sqrt{1 - PF^*} \tag{B.34}$$

being PF^* the power factor reference, q^* the reference applied to the reactive power controller, and p the real active power measured in PCC. Although the power factor is a variable that has no sign, in this case a sign will be added to it in order to discriminate both operation modes. In this way sign '+' indicates capacitive behavior, and '-' indicates inductive mode.

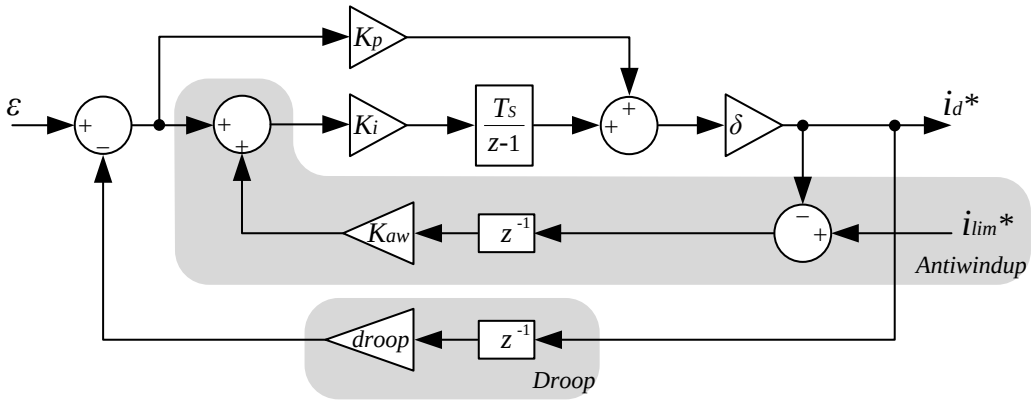


Figure B.16. PCC voltage controller.

Appendix C: INDUCTION MACHINE DESCRIPTION AND CONTROL

The widely extended use of induction machines (IM), especially the squirrel-cage motors, in the industry is due to their ruggedness and simplicity. For this reason the induction motor drives dominate the world market. Then, the challenge is design a control structure for the induction machine, having into account that the rotor currents or the rotor flux in a squirrel-cage motor cannot be directly monitored and the stator field rotation speed can be different to the rotor speed.

In general terms, an asynchronous machine can be considered as a transformer where the secondary winding (rotor) is mounted on mechanical bearings, and rotates inside the primary winding (stator) leaving between them an airgap.

The stator consists basically of several coils embedded in the slots of a magnetic core. In general, all the coils are identical and the span between them is called the pole pitch. The number of poles can be defined as the number of times that a single phase is repeated along the periphery of the stator. In every pole there are three zones, one per phase, where one or several slots per phase can be found.

Regarding the rotor topology, two kind of IM can be taken into account. The squirrel cage IM consists of a laminated core with uniform bars short-circuited by end-rings, while a wound rotor IM is provided of three-phase windings (as in stator) connected to some copper rings and fixed brushes. It have been demonstrated that a symmetric cage with round bars can be modelled as a three-phase winding. Hence, these two types of IM rotor are equivalent.

In this section the mathematical model of an induction machine will be explained, and also the controllers used in this work.

C.1. Asynchronous machine mathematical model

The main expression within the mathematical model of an induction machine is the voltage-current equation. In (C.1) this expression reduced to the stator is represented using matrix form and *abc*-reference frames. Note that to reduce a rotor variable to the stator only is needed to use the transformer equivalent ratio between rotor and stator windings. The variables with an *s* subscript are related to the stator and those with *r* related with the rotor.

$$[V] = [r][i] + [e]$$
$$[e] = \frac{d[\lambda]}{dt}$$
$$[\lambda] = [L(\theta_{er})][i]$$
$$[r] = \begin{bmatrix} r_s & 0 & 0 & 0 & 0 & 0 \\ 0 & r_s & 0 & 0 & 0 & 0 \\ 0 & 0 & r_s & 0 & 0 & 0 \\ 0 & 0 & 0 & r_r & 0 & 0 \\ 0 & 0 & 0 & 0 & r_r & 0 \\ 0 & 0 & 0 & 0 & 0 & r_r \end{bmatrix} \quad [V] = \begin{bmatrix} V_{as} \\ V_{bs} \\ V_{cs} \\ V_{ar} \\ V_{br} \\ V_{cr} \end{bmatrix} \quad [i] = \begin{bmatrix} i_{as} \\ i_{bs} \\ i_{cs} \\ i_{ar} \\ i_{br} \\ i_{cr} \end{bmatrix} \quad [\lambda] = \begin{bmatrix} \lambda_{as} \\ \lambda_{bs} \\ \lambda_{cs} \\ \lambda_{ar} \\ \lambda_{br} \\ \lambda_{cr} \end{bmatrix} \tag{C.1}$$

In (C.1) $[V]$ is the voltage matrix, $[i]$ the current matrix, $[\lambda]$ the flux linkages matrix, and $[e]$ is the back electromotive force (EMF) matrix. $[L(\theta_{er})]$ is the inductance matrix:

$$[L(\theta_{er})] = \begin{bmatrix} L_{ss}^{abc} & L_{sr}^{abc} \\ L_{rs}^{abc} & L_{rr}^{abc} \end{bmatrix}_{6x6}$$
$$[L_{ss}^{abc}] = \begin{bmatrix} L_{ls}+L_{ss} & L_{sm} & L_{sm} \\ L_{sm} & L_{ls}+L_{ss} & L_{sm} \\ L_{sm} & L_{sm} & L_{ls}+L_{ss} \end{bmatrix} \quad [L_{rr}^{abc}] = \begin{bmatrix} L_{lr}+L_{rr} & L_{rm} & L_{rm} \\ L_{rm} & L_{lr}+L_{rr} & L_{rm} \\ L_{rm} & L_{rm} & L_{lr}+L_{rr} \end{bmatrix} \tag{C.2}$$
$$[L_{sr}^{abc}] = [L_{rs}^{abc}]^T = L_{sr} \begin{bmatrix} \cos(\theta_{er}) & \cos(\theta_{er}+\frac{2\pi}{3}) & \cos(\theta_{er}-\frac{2\pi}{3}) \\ \cos(\theta_{er}-\frac{2\pi}{3}) & \cos(\theta_{er}) & \cos(\theta_{er}+\frac{2\pi}{3}) \\ \cos(\theta_{er}+\frac{2\pi}{3}) & \cos(\theta_{er}-\frac{2\pi}{3}) & \cos(\theta_{er}) \end{bmatrix}$$

where L_{ls} and L_{lr} are the stator and rotor winding leakage inductances per phase, L_{ss} and L_{rr} are the self-inductance of the stator and rotor windings, respectively, and L_{sr} is the peak value of the stator-to-rotor mutual inductance.

Replacing the EMF in (C.1) by the time derivative of the flux linkage it is obtained the following expression:

$$[V] = [r][i] + \frac{d[\lambda]}{dt} = [r][i] + [L(\theta_{er})]\frac{d[i]}{dt} + \frac{d[L(\theta_{er})]}{d\theta_{er}}[i]\frac{d\theta_{er}}{dt} \tag{C.3}$$

In this way a 6th order nonlinear model with time-varying coefficients has been obtained. This is due to the inductance matrix depends on the electrical rotor position.

The previous model is not very used because of the high computation effort that it implies; instead the model in *dq*-reference frame is used as it achieves constant values for the inductances. The *abc* three-phase to *ω*-rotating reference frame (*dqω*) is defined as

$$T_{abc\to dq}(\theta) = \frac{2}{3}\begin{bmatrix} \cos(\theta) & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ -\sin(\theta) & -\sin\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) \end{bmatrix} \tag{C.4}$$

where $\theta = \frac{d\omega}{dt}$. And the pseudo inverse matrix $T_{dq\to abc}(\theta)$ is

$$T_{dq\to abc}(\theta) = \begin{bmatrix} \cos(\theta) & -\sin(\theta) \\ \cos\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta - \frac{2\pi}{3}\right) \\ \cos\left(\theta + \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) \end{bmatrix} \tag{C.5}$$

In this way, the stator voltage of equation (C.3) can be rewritten in *dqω* as:

$$[V_{dq\omega s}] = [T_{abc\to dq}(\theta)]\left([r_s][T_{dq\to abc}(\theta)][i_{dq\omega s}] + \frac{d([T_{dq\to abc}(\theta)][\lambda_{dq\omega s}])}{dt}\right) \tag{C.6}$$

The time-derivative term may be expressed as:

$$\frac{d([T_{dq\to abc}(\theta)][\lambda_{dq\omega s}])}{dt} = \omega\frac{d([T_{dq\to abc}(\theta)])}{d\theta}[\lambda_{dq\omega s}] + [T_{dq\to abc}(\theta)]\frac{d([\lambda_{dq\omega s}])}{dt} \tag{C.7}$$

Replacing (C.6) into (C.7) and rearranging, the following expression is obtained:

$$[V_{dq\omega s}] = [r_s][i_{dq\omega s}] + \frac{d([\lambda_{dq\omega s}])}{dt} + \omega\begin{bmatrix} 0 & 1 \\ -1 & 0 \end{bmatrix}[\lambda_{dq\omega s}] \tag{C.8}$$

where $[r_s]$ is the stator resistance matrix:

$$[r_s] = \begin{bmatrix} r_s & 0 \\ 0 & r_s \end{bmatrix} \tag{C.9}$$

Figure C.1 shows the angle shift that exists between the stator and rotor *abc*-axis. This angle must be taken into account when referring rotor variables into other reference frames. According to this and following the same procedure as in the case of the stator, the rotor voltage expression is:

$$[V_{dq\omega r}] = [r_r][i_{dq\omega r}] + \frac{d([\lambda_{dq\omega r}])}{dt} + (\omega - \omega_{er})\begin{bmatrix} 0 & 1 \\ -1 & 0 \end{bmatrix}[\lambda_{dq\omega r}] \tag{C.10}$$

where ω_{er} is the electrical rotor speed and $[r_r]$ is the rotor resistance matrix:

$$\frac{d\omega_{er}}{dt} = \theta_{er} \tag{C.11}$$

$$[r_r] = \begin{bmatrix} r_r & 0 \\ 0 & r_r \end{bmatrix} \tag{C.12}$$

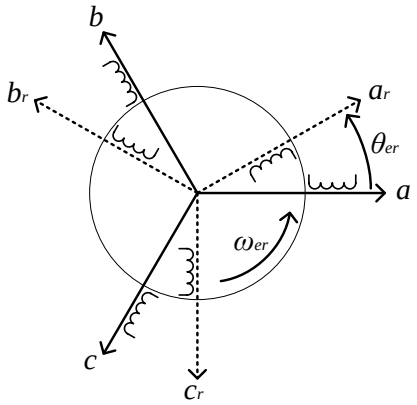


Figure C.1. Rotor and stator diagram in abc-frames.

On the other hand, the stator flux expression in *dqω* is:

$$[\lambda_{dq\omega s}] = [T_{abc\to dq}(\theta)][L_{ss}^{abc}][T_{dq\to abc}(\theta)][i_{dq\omega s}] + [T_{abc\to dq}(\theta)][L_{sr}^{abc}][T_{dq\to abc}(\theta - \theta_{er})][i_{dq\omega r}] \tag{C.13}$$

Or expressed in other way:

$$[\lambda_{dq\omega s}] = \begin{bmatrix} L_{ls} + L_m & 0 \\ 0 & L_{ls} + L_m \end{bmatrix}[i_{dq\omega s}] + \begin{bmatrix} L_m & 0 \\ 0 & L_m \end{bmatrix}[i_{dq\omega r}] \tag{C.14}$$

where L_m is the magnetizing inductance. Remember that all rotor quantities are referred to the stator winding through the transformer equivalent ratio:

$$L_m = \frac{3}{2}L_{ss} = \frac{3}{2}L_{sr} = \frac{3}{2}L_{rr} \tag{C.15}$$

In a similar way, the *dqω* rotor flux expression is given by:

$$\begin{aligned}\left[\lambda_{dq\omega r}\right] = &\left[T_{abc\to dq}(\theta)\right]\left[L_{rs}^{abc}\right]\left[T_{dq\to abc}(\theta)\right]\left[i_{dq\omega s}\right] \\ &+ \left[T_{abc\to dq}(\theta)\right]\left[L_{rr}^{abc}\right]\left[T_{dq\to abc}(\theta-\theta_{er})\right]\left[i_{dq\omega r}\right]\end{aligned} \tag{C.16}$$

or:

$$\left[\lambda_{dq\omega r}\right] = \begin{bmatrix} L_m & 0 \\ 0 & L_m \end{bmatrix}\left[i_{dq\omega s}\right] + \begin{bmatrix} L_{lr}+L_m & 0 \\ 0 & L_{lr}+L_m \end{bmatrix}\left[i_{dq\omega r}\right] \tag{C.17}$$

As it can be seen, in the previous expressions all parameters are time invariant and now only two axes are taken into account instead of three. This fact easies the induction machine analysis.

In the case that ω is zero the obtained reference frame is known as stationary reference frame. Substituting the value $\omega = 0$ in the equations (C.8) and (C.10), the following expressions can be obtained:

$$\begin{aligned} V_{\alpha s} &= r_s i_{\alpha s} + \frac{d\lambda_{\alpha s}}{dt} & V_{\beta s} &= r_s i_{\beta s} + \frac{d\lambda_{\beta s}}{dt} \\ \lambda_{\alpha s} &= L_s i_{\alpha s} + L_m i_{\alpha r} & \lambda_{\beta s} &= L_s i_{\beta s} + L_m i_{\beta r} \\ V_{\alpha r} &= r_r i_{\alpha r} + \frac{d\lambda_{\alpha r}}{dt} + \omega_{er}\lambda_{\beta r} & V_{\beta r} &= r_r i_{\beta r} + \frac{d\lambda_{\beta r}}{dt} - \omega_{er}\lambda_{\alpha r} \\ \lambda_{\alpha r} &= L_r i_{\alpha r} + L_m i_{\alpha s} & \lambda_{\beta r} &= L_r i_{\beta r} + L_m i_{\beta s} \end{aligned} \tag{C.18}$$

where L_s and L_r are the stator and rotor inductances respectively:

$$\begin{aligned} L_s &= L_{ls} + L_m \\ L_r &= L_{lr} + L_m \end{aligned} \tag{C.19}$$

The induction machine model in synchronous reference frame is obtained when ω matches up with the stator excitation frequency ω_e, turning the *dqω* reference frame into *dq*:

$$\begin{aligned} V_{ds} &= r_s i_{ds} + \frac{d\lambda_{ds}}{dt} - \omega_e\lambda_{qs} & V_{qs} &= r_s i_{qs} + \frac{d\lambda_{qs}}{dt} + \omega_e\lambda_{ds} \\ \lambda_{ds} &= L_s i_{ds} + L_m i_{dr} & \lambda_{qs} &= L_s i_{qs} + L_m i_{qr} \\ V_{dr} &= r_r i_{dr} + \frac{d\lambda_{dr}}{dt} - (\omega_e - \omega_{er})\lambda_{qr} & V_{qr} &= r_r i_{qr} + \frac{d\lambda_{qr}}{dt} + (\omega_e - \omega_{er})\lambda_{dr} \\ \lambda_{dr} &= L_r i_{dr} + L_m i_{ds} & \lambda_{qr} &= L_r i_{qr} + L_m i_{qs} \end{aligned} \tag{C.20}$$

In such conditions, Figure C.2 shows the induction machine equivalent circuit in synchronous reference frames described in (C.20). The factors included in *d*-axis circuit and belong to *q*-axis and vice versa are introduced as dependent voltage sources.

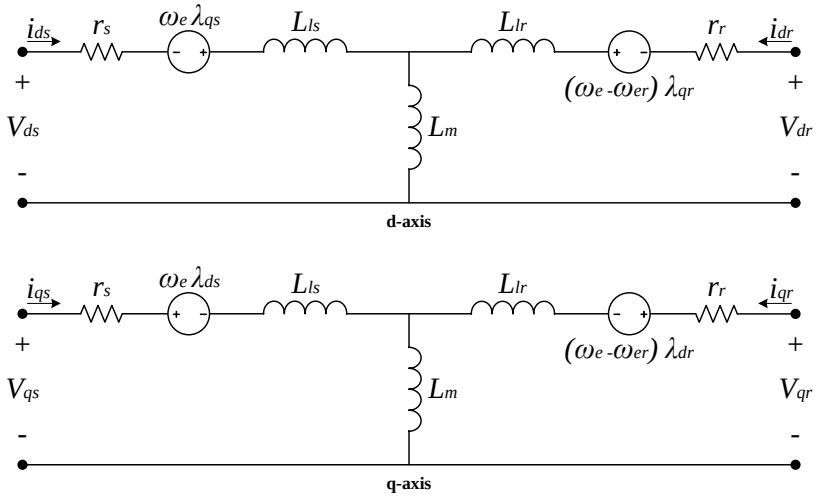


Figure C.2. Induction machine equivalent circuit in synchronous reference frames.

In induction machines the torque is defined as the tendency of a force to rotate an object (the load) around and axis (the rotor). In this it will be used the following expression for the machine torque:

$$T_{em} = \frac{3}{2}p\left(\lambda_{ds}i_{qs} - \lambda_{qs}i_{ds}\right) = \frac{3}{2}p\left(\lambda_{qr}i_{dr} - \lambda_{dr}i_{qr}\right) = \frac{3}{2}pL_m\left(i_{qs}i_{dr} - i_{ds}i_{qr}\right) \tag{C.21}$$

Where p is the number of pole pairs.

On the other hand, the power that the machine may develop is:

$$P_{em} = T_e\omega_{mr} \tag{C.22}$$

Being ω_{mr} the mechanical rotor speed:

$$\omega_{mr} = \frac{\omega_{er}}{p} \tag{C.23}$$

When a variation is produced in the vector product of two flux linkages, a torque is generated to create opposition to that variation. In the case of induction machines, there are two flux linkages: one in stator and the other in rotor. If the rotation speed of the rotor flux (ω_{er}) is different from stator one (ω_e), the vector product between both fluxes varies and a torque is developed. The difference between both speeds is known as slip speed, ω_s, and a then the ratio known as slip can be defined:

$$s = \frac{\omega_e - \omega_{er}}{\omega_e} = \frac{\omega_s}{\omega_e} \tag{C.24}$$

The slip ratio gives information about the developed torque and power. Moreover, it could be used to know the machine working mode. Attending to this objective, in order to

relate the power and torque with the slip the machine model is analyzed in steady state. In these conditions, the voltage equations in (C.18) can be expressed as:

$$\begin{aligned} V_{\alpha s} &= r_s i_{\alpha s} + j\omega_e (L_s i_{\alpha s} + L_m i_{\alpha r}) \\ V_{\alpha r} &= r_r i_{\alpha r} + j\omega_e (L_r i_{\alpha r} + L_m i_{\alpha s}) + \omega_{er} \left(L_r i_{\beta r} + L_m i_{\beta s}\right) \\ V_{\beta s} &= r_s i_{\beta s} + j\omega_e \left(L_s i_{\beta s} + L_m i_{\beta r}\right) \\ V_{\beta r} &= r_r i_{\beta r} + j\omega_e \left(L_r i_{\beta r} + L_m i_{\beta s}\right) - \omega_{er} (L_r i_{\alpha r} + L_m i_{\alpha s}) \end{aligned} \tag{C.25}$$

If a space-vector notation ($\vec{X}_{\alpha\beta} = X_\alpha + jX_\beta$) is used, the equations in (C.25) can be rewritten as follows:

$$\begin{aligned} \vec{V}_{\alpha\beta s} &= (r_s + j\omega_e L_s)\vec{i}_{\alpha\beta s} + j\omega_e L_m \vec{i}_{\alpha\beta r} \\ \vec{V}_{\alpha\beta r} &= (r_r + js\omega_e L_r)\vec{i}_{\alpha\beta r} + js\omega_e L_m \vec{i}_{\alpha\beta s} \end{aligned} \tag{C.26}$$

The α-axis component matches up with the a-axis component. Taking into account this consideration, if the rotor voltage equation is divided by the slip and rearranging terms using (C.19), the following expression is obtained:

$$\begin{aligned} V_{as} &= r_s i_{as} + j\omega_e L_{ls} i_{as} + j\omega_e L_m (i_{as} + i_{ar}) \\ \frac{V_{ar}}{s} &= \frac{r_r}{s} i_{ar} + j\omega_e L_{lr} i_{ar} + j\omega_e L_m (i_{as} + i_{ar}) \end{aligned} \tag{C.27}$$

According to equation (C.27), Figure C.3 represents the induction machine equivalent circuit in stationary reference frames. When the rotor resistance is separated out, the remaining term $r_r(1-s)/s$ may be associated with the developed mechanical power, whereas the resistor r_r/s is associated with the power through the airgap. Therefore, in steady state, the developed power average value is [130]:

$$P_{em} = 3\, {i_{ar}}^2\, \frac{1-s}{s}\, r_r \tag{C.28}$$

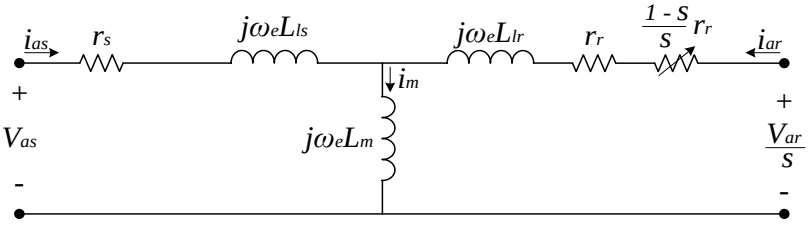


Figure C.3. Induction machine a-axis equivalent circuit in steady state

An alternative expression for the developed electromagnetic torque can be derived from equation (C.28):

$$T_{em} = \frac{P_{em}}{\omega_{mr}} = \frac{3\ p\ {i_{ar}}^2\ r_r}{\omega_s - \omega_{er}} \tag{C.29}$$

In order to obtain a relationship between the torque and the slip, the Thevenin's equivalent can be applied in the circuit of Figure C.3, obtaining the circuit shown in Figure C.4 and the following expressions:

$$\begin{aligned} V_{th} &= \frac{j\omega_e L_m}{r_s + j\omega_e(L_{ls} + L_m)} V_{as} \\ Z_{th} = r_{th} + jx_{th} &= \frac{j\omega_e L_m (r_s + j\omega_e L_{ls})}{r_s + j\omega_e(L_{ls} + L_m)} \end{aligned} \tag{C.30}$$

In function of the Thevenin's circuit parameters, the average value of the electromagnetic torque developed with constant voltage supply has the following expression:

$$T_{em} = \frac{3p}{\omega_e} \frac{{V_{th}}^2\ \frac{r_r}{s}}{\left(r_{th} + \frac{r_r}{s}\right)^2 + (x_{th} + x_{lr})^2} \tag{C.31}$$

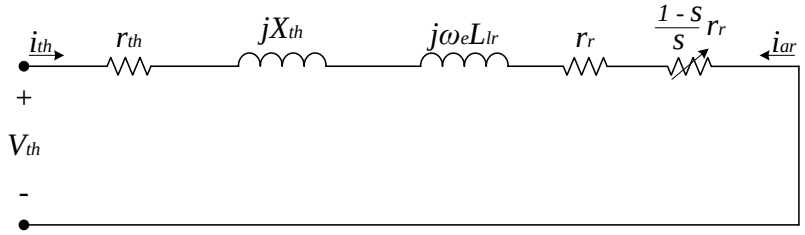


Figure C.4. Thevening's equivalent of the stator when the rotor windings are short-circuited.

Based on equation (C.31), Figure C.5 shows the torque variation as a function of the slip. The torque is null if no slip is produced in the machine. Besides, if the slip is positive the machine works as a motor while if it is negative the machine works as a generator.

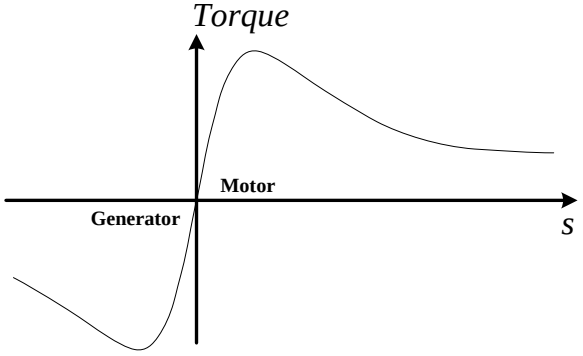


Figure C.5. Average torque as a function of the slip, having constant voltage supply.

As it can be seen in Figure C.5, when the machine works as a generator the electromagnetic torque is negative, and if it works as a motor the torque is positive. In the first case the rotor speed is higher than the stator frequency, and the opposite happens in the motor case. The maximum torque achieved by the machine must be developed when the machine starts its movement.

Until this point the electromagnetic part of an induction machine has been mathematically described. Equation (C.32) shows the mechanical behavior of every rotating machine. This expression indicates the evolution of the rotor speed as a function of the difference between the developed and load torques. The inertia of the rotor is represented as *J*.

$$\frac{J}{p}\frac{d\omega_e}{dt} = T_{em} - T_{mech} \tag{C.32}$$

C.2. Vector control of an induction machine

The reason why the vector control is used in induction machine is that it allows controlling independently flux and torque with the two components of the synchronous reference frame stator current. Due to the flux dynamic response is slow, it is usually forced to be constant in order to avoid core saturation through flux weakening, while fast response is achieved in torque and speed.

To make possible the induction machine control a voltage source converter (VSC) is used. In this way, the vector control will have as output signal a voltage reference that will be use to modulate the VSC. The voltage reference will be used to generate pulse-with modulated signals for the converter though a modulation method.

As the squirrel-cage induction machine is de most commonly used in industry, the control will be described for this kind of machine. Hence, the rotor windings are short-circuited. The idea is to synchronize the *d*-axis with the rotor flux, and this is why vector control is also called field oriented control (FOC). There are several techniques to implementing the FOC in induction machines [130][131], and they can be divided into two categories: direct and indirect FOC.

In direct field oriented control schemes the rotor flux angle is calculated by measuring the airgap flux. Besides, in these schemes the converter can be controlled through stator current or stator voltage references. So, we can distinguish between direct field oriented current control and direct FOC voltage control [130]. Both control schemes are represented respectively in Figure C.6.a and Figure C.6.b.

The drift in the integrator associated with the flux sensor is especially problematic at very low frequency. Moreover, these control techniques usually employ hysteresis controllers. This implies a non-linear controller with high ripple over the responses. Instead of the previous method, the flux orientation can be obtained by measuring the currents and the rotor

position [130]. This is known as indirect field orientation control, and this is the method used in this case. A representation of this method appears in Figure C.7.

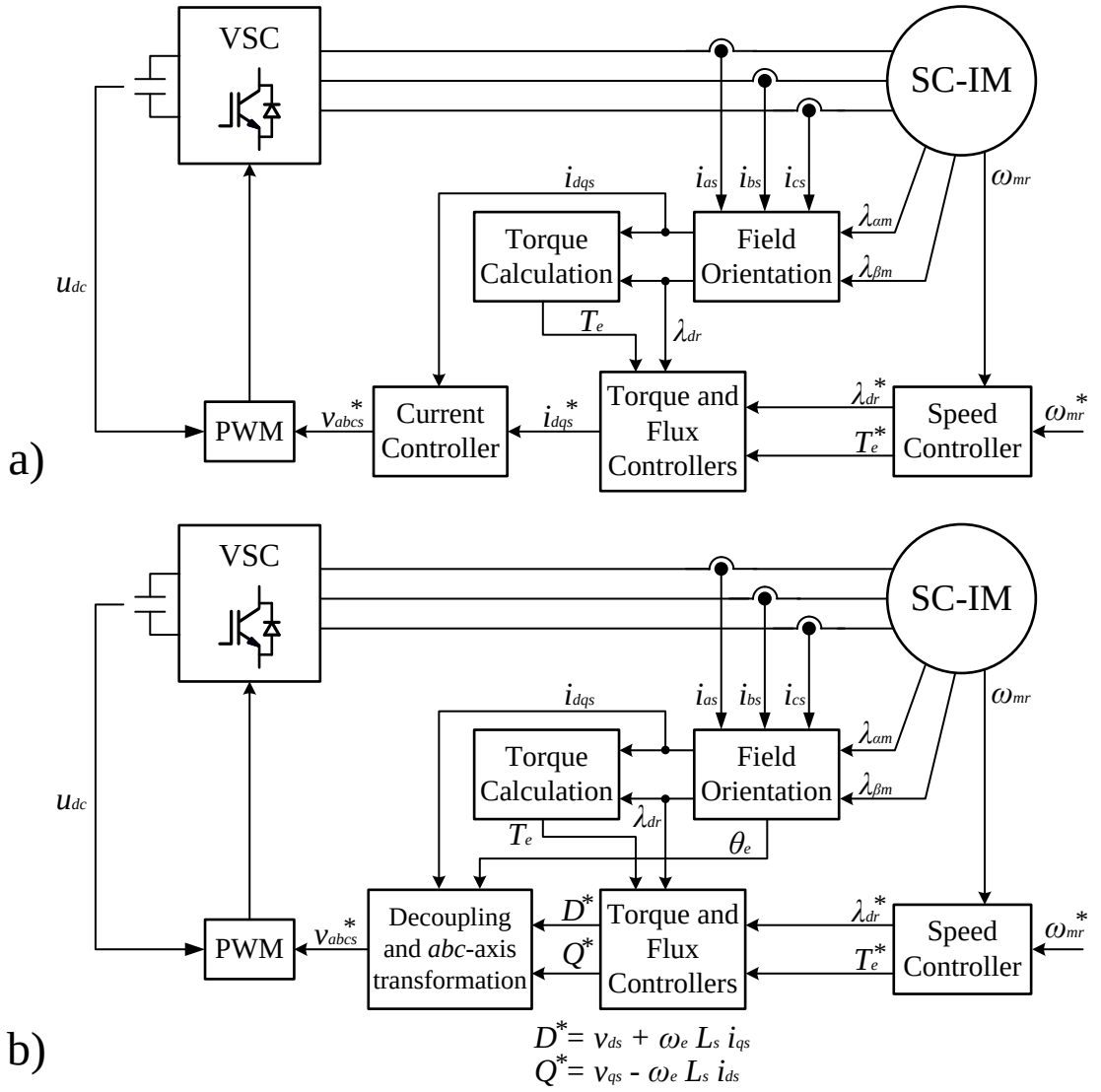


Figure C.6. Direct field oriented current control (a); and Direct field oriented voltage control (b).

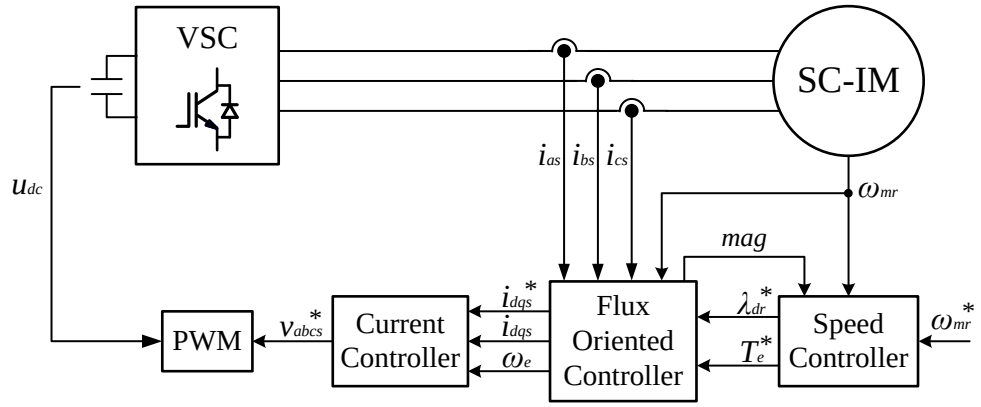


Figure C.7. Indirect field oriented control.

As it is shown in Figure C.7, there are three main blocks in the indirect field oriented control: the speed control, the flux oriented control, and the current control. These three controllers will be explained separately in next subsections.

As the general idea of the indirect flux oriented control is to synchronize the rotor flux with the *d*-axis, if this synchronization is achieved the *q*-axis flux component should be null (see Figure C.8). From (C.20) the following statement can be obtained:

$$\lambda_{qr} = L_m i_{qs} + L_r i_{qr} = 0 \quad \rightarrow \quad i_{qr} = -\frac{L_m}{L_r} i_{qs} \tag{C.33}$$

If the rotor current *q*-component (C.33) is substituted in the torque equation (C.21) the following expression is obtained:

$$T_{em} = \frac{3}{2} p \frac{L_m}{L_r} \lambda_{dr} i_{qs} \tag{C.34}$$

Considering equation (C.34) we can see that if the rotor flux is not disturbed, the toque can be independently controlled though the stator current *q*-component. Besides, if a permanent perfect synchronization is desired, λ_{qr} must remain invariable, what is assured it its time derivative is null:

$$\frac{d\lambda_{qr}}{dt} = 0 \tag{C.35}$$

As the torque must be controlled by i_{qs}, the *d*-axis flux linkage must be constant in steady state. Hence, its time derivative is considered null too. The slip speed value is obtained from the *q*-axis rotor voltage expression (C.20):

$$\begin{gathered} \underbrace{V_{qr}}_{0} = r_r i_{qr} + \underbrace{\frac{d\lambda_{qr}}{dt}}_{0} + (\omega_e - \omega_{er})\lambda_{dr} \\ \omega_s = \omega_e - \omega_{er} = -\frac{r_r i_{qr}}{\lambda_{dr}} \end{gathered} \tag{C.36}$$

And from the *d*-axis rotor voltage equation (C.20) it can be obtained the following:

$$\begin{gathered} \underbrace{V_{dr}}_{0} = r_r i_{dr} + \underbrace{\frac{d\lambda_{dr}}{dt}}_{0} - (\omega_e - \omega_{er}) \underbrace{\lambda_{qr}}_{0} \\ i_{dr} = 0 \end{gathered} \tag{C.37}$$

Thus, in steady state it must be satisfied the following expression:

$$\lambda_{dr} = L_m i_{ds} \tag{C.38}$$

what indicates that the rotor flux amplitude can be controlled through i_{ds}. Substituting (C.38) in equation (C.36) and rearranging, the slip speed can be expressed as a function of the ratio between the stator current components in synchronous reference frame:

$$\omega_s = \frac{r_r i_{qs}}{L_r i_{ds}} \tag{C.39}$$

Therefore, the rotor flux amplitude can be adjusted through the *d*-axis stator current, and its orientation will be maintained by the slip speed or indirectly by the *q*-axis stator current, which controls the torque too. With the proper field orientation, the dynamics of λ_{dr} will be confined to the d-axis and are determined by the rotor circuit time constant, τ:

$$\tau = \frac{L_r}{r_r} \tag{C.40}$$

From equations (C.20) and (C.37), we have that in transients the *d*-axis rotor flux is:

$$\lambda_{dr} = -\frac{r_r i_{dr}}{S} = \frac{r_r L_m}{r_r + L_r S} i_{ds} \tag{C.41}$$

Note that in equation (C.41) *S* does not represent the slip, but the Laplace operator (*d*/*dt*).

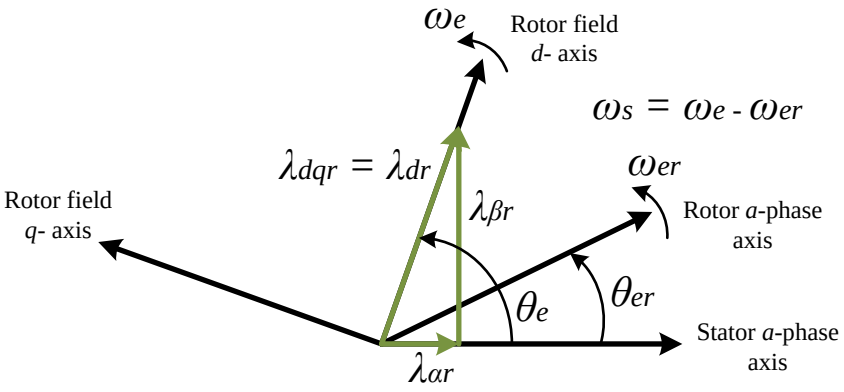


Figure C.8. Flux-oriented control vector diagram.

Considering all the above explained, the control loop is designed. As it have been mentioned, it is composed by three controllers connected in series inside the control loop: the output of a controller is the input for the following one. It is evident that the dynamics of each of them will affect the rest, so, in order to reduce the influence of one controller over the rest, the response time of each one must be configured carefully.

The current controller is the most internal of the three inside the loop, so, it has to be set fast enough to not be considered as an influence over the external controllers. The flux oriented controller is in middle, and its settling time has to be bigger than the current controller and smaller than the speed controller. Thus, the speed controller has to be the slowest one of the three in the control loop, in order to avoid interferences in the dynamics between controllers.

For the controllers tuning the following steps are carried out:

- Obtain the plant transfer function in Laplace domain through the mathematical model presented previously.

- Transform the transfer function into the discrete *Z*-domain due to the final objective is to design controllers to be implemented in a digital platform.

- Calculate the closed-loop transfer function that is composed by the obtained discrete plant and the controller. In this case, the used controllers are proportional-integral (PI).

- Once the closed-loop transfer function is obtained, its denominator is used to calculate the PI controller constants in function of the settling time (t_s) and the overshoot (represented by the overshoot factor, ξ) through a comparison with the a second order standard system denominator:

$$D(z) = z^2 - 2\rho \cos\theta \, z + \rho^2 \tag{C.42}$$

where $= \omega_n\sqrt{1-\xi^2}\,T_s$, $\rho = e^{-\omega_n \xi T_s}$, and $\omega_n = f(t_s)$. The overshoot factor is usually configured as $\xi = {}^{1}/_{\sqrt{2}} \approx 0.7071$.

In the following subsections each controller is explained separately.

C.2.2. Speed controller

The speed controller must meet the following requirements:

- Speed rate limiter. Too high acceleration references are not allowed by the control because enormous current peaks can appear causing serious damages on the power converter.

- Flux reference. In order to not get saturation condition on the machine, the flux reference is limited when rotor speed reaches high values. This is called 'Field Weakening'. In this way, the system voltage limit is more difficult to get reached.

- Torque reference. The main goal of the speed controller is to make the rotor speed follows its reference. For this purpose, a PI controller is used, whose output is limited to avoid undesirable torque references.

- Magnetization of the machine. At the start-up, all induction machine need to be magnetized. The speed controller contributes to this progress avoiding the start-up of the machine. To that effect, null speed reference and maximum flux reference are supplied.

According to the previously explained, Figure C.9 shows the speed controller block diagram.

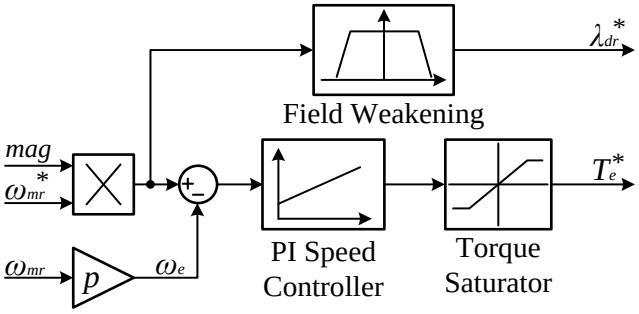


Figure C.9. Speed controller block diagram.

In the case of this controller the transfer function is obtained from the mechanical model described in equation (C.32):

$$T_\omega(S) = \frac{\omega_r}{T_e}(S) = \frac{p}{JS} \tag{C.43}$$

Where *S* is the Laplace operator, and if the ZOH method is applied to discretize the plant:

$$T_\omega(z) = \frac{pT_s}{J}\frac{1}{z-1} \tag{C.44}$$

On the other hand, the speed PI controller transfer function is given by:

$$C_\omega(z) = k_{p\omega}\frac{z-\alpha_\omega}{z-1} \tag{C.45}$$

So, the closed loop transfer function for the speed controller is:

$$H_\omega(z) = \frac{CT_\omega(z)}{1+CT_\omega(z)} = \frac{pT_s k_{p\omega}}{J}\frac{z-\alpha_\omega}{z^2-\left(2-\frac{pT_s k_{p\omega}}{J}\right)z+1-\frac{pT_s k_{p\omega}}{J}\alpha_\omega} \tag{C.46}$$

Comparing the denominator in (C.46) with the second order standard system denominator (C.42), as it has been mentioned previously, the controller's constants can be calculated:

$$k_{p\omega} = \frac{2J}{pT_s}\left[1 - e^{-\omega_n \xi T_s}\cos\left(\omega_n\sqrt{1-\xi^2}\,T_s\right)\right]$$
$$\alpha_\omega = \frac{1}{2}\frac{1 - e^{-2\omega_n \xi T_s}}{1 - e^{-\omega_n \xi T_s}\cos\left(\omega_n\sqrt{1-\xi^2}\,T_s\right)} \tag{C.47}$$
$$k_{i\omega} = \frac{k_{p\omega}}{T_s}(1 - \alpha_\omega)$$

where $k_{p\omega}$, α_ω, and $k_{i\omega}$ are the proportional constant, the zero, and the integral constant of the PI controller respectively.

In Figure C.9 it can also be seen an input signal called *mag* that makes null the speed reference while a certain level of the rotor flux is not reached, i.e. while the machine is being magnetized.

C.2.3. Flux oriented controller

As it was mentioned, the vector control main task is to provide independent controls for flux and torque. Figure C.10 shows the flux oriented control block diagram, that is composed by the stator frequency and phase calculation, the flux calculation, and the flux controller. This controller obtains the current components in synchronous reference frames as well as their references. As there are not flux linkage measures, it is an indirect FOC, where the synchronization between the rotor flux and the *d*-axis is done following expressions (C.33) and (C.41).

The first step is calculating the current *dq*-components, that are obtained though the transformation matrix $T_{abc\rightarrow dq}(\theta_e)$ (equation (C.4)). Then, the rotor *d*-axis flux is calculated using the ZOH discrete version of equation (C.41). Once both currents and flux are obtained, the electrical stator frequency and phase are calculated through equation (C.39), and it is then when the loop can be closed.

According to (C.34), and using the torque reference supplied by the speed controller and the flux calculated, the *q*-axis reference current is obtained. As mentioned before, this component is used to control the torque.

The flux controller implemented consists on a PI controller and a saturator with anti-windup. Its output is used to calculate the *d*-axis component of the current. The controller constants are calculated similarly to the previous controller. First of all, the plant transfer function is obtained from equation (C.41):

$$T_f(S) = \frac{\lambda_{dr}}{i_{ds}}(S) = \frac{r_r L_m}{r_r + L_r S} \tag{C.48}$$

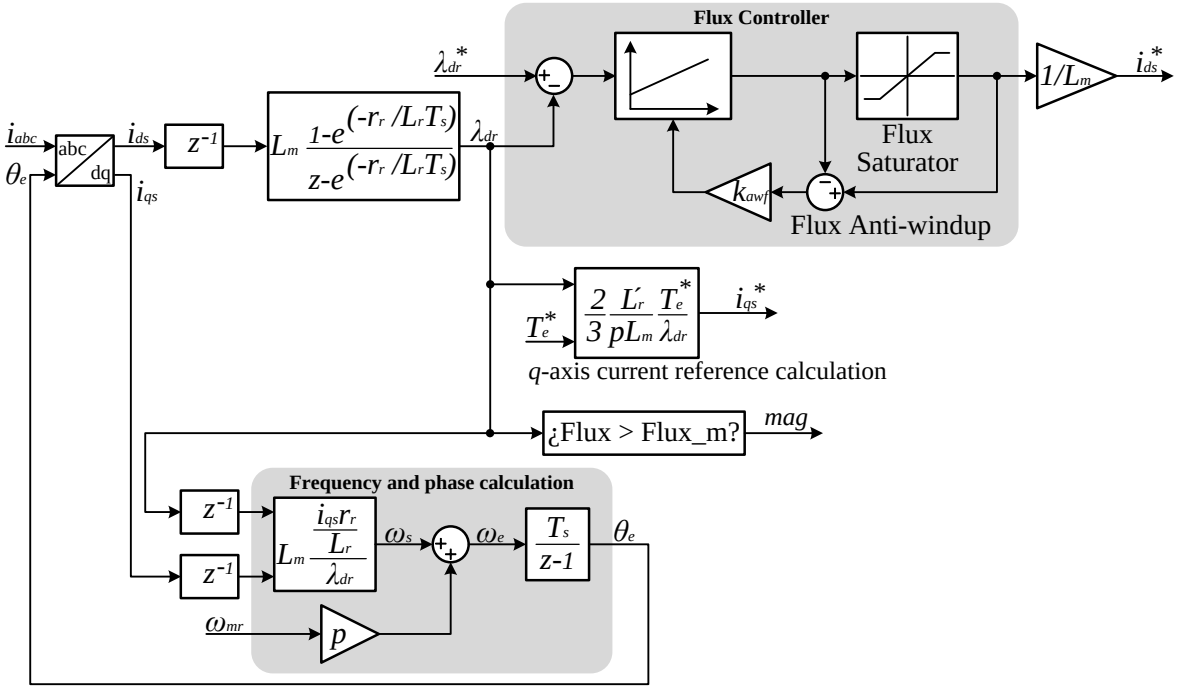


Figure C.10. Indirect flux oriented controller block diagram.

The transfer function in discrete time domain is given by:

$$T_f(z) = L_m \frac{1 - e^{\frac{r_r}{L_r}T_s}}{z - e^{\frac{r_r}{L_r}T_s}} = \frac{a_f}{z + b_f} \tag{C.49}$$

So, the closed loop transfer function is:

$$H_f(z) = \frac{CT_f(z)}{1 + CT_f(z)} = a_f k_{pf} \frac{z - \alpha_f}{z^2 - \left(b_f + 1 - a_f k_{pf}\right)z + b_f - a_f k_{pf}\alpha_f} \tag{C.50}$$

Comparing the closed loop transfer function denominator (C.50) with the second order standard system denominator (C.42), the controller's constants can be calculated:

$$\begin{aligned} k_{pf} &= \frac{b_f + 1 - 2e^{-\omega_n \xi T_s}\cos\left(\omega_n\sqrt{1-\xi^2}\,T_s\right)}{a_f} \\ \alpha_f &= \frac{b_f - e^{-2\omega_n \xi T_s}}{b_f + 1 - e^{-\omega_n \xi T_s}\cos\left(\omega_n\sqrt{1-\xi^2}\,T_s\right)} \end{aligned} \tag{C.51}$$

$$k_{if} = \frac{k_{pf}}{T_s}(1 - \alpha_f)$$

The anti-windup gain is chosen as:

$$k_{af} = \frac{1}{k_{pf}} \tag{C.52}$$

The settling time of this controller must be configured lower than the speed controller one, but higher than the current controller settling time. In this way the interference between controllers is minimized.

On the other hand, the *mag* signal is generated in this controller depending on the rotor flux magnitude: when a certain value is reached, *mag* enables the speed controller to supply torque references. Hence, if the machine is magnetized enough, the control gives command to start moving the rotor.

C.2.4. Current controller

The current controller objective is making both stator current components follow their respective references in order to obtain zero current error. There are several techniques for implementing the current control in a power electronic converter, but in this case a linear controller will be used where the current errors are integrated by PIs and a sine-triangle PWM is obtained.

Figure C.11 shows the current controller block diagram that consist on a *q*-axis current reference saturator, a *dq*-axis current controllers with anti-windup, a *dq*-axis voltage saturator, and a PWM modulator. However, the PWM modulator does not properly belong to the current controller.

All the inputs for the current controller are supplied by the flux oriented controller. As mentioned before, the *q*-axis current reference is saturated, so the magnitude of the vector i_{dq}^* must satisfy the following condition:

$$\left|\vec{i}_{dqs}^{\,*}\right| = \sqrt{(i_{ds}^{\,*})^2 + \left(i_{qs}^{\,*}\right)^2} \leq \frac{S_n}{V_n} \tag{C.53}$$

where S_n is the AC driver rated apparent power in VAr, and V_n is the stator rated voltage in V_{rms}. From (C.53):

$$i_{qs}'^{*} \leq \sqrt{\left(\frac{S_n}{V_n}\right)^2 - (i_{ds}^{\,*})^2} \tag{C.54}$$

where $i_{qs}^{'*}$ is the saturated version of i_{qs}^{*}. It must be noted that only the component that controls the toque is limited.

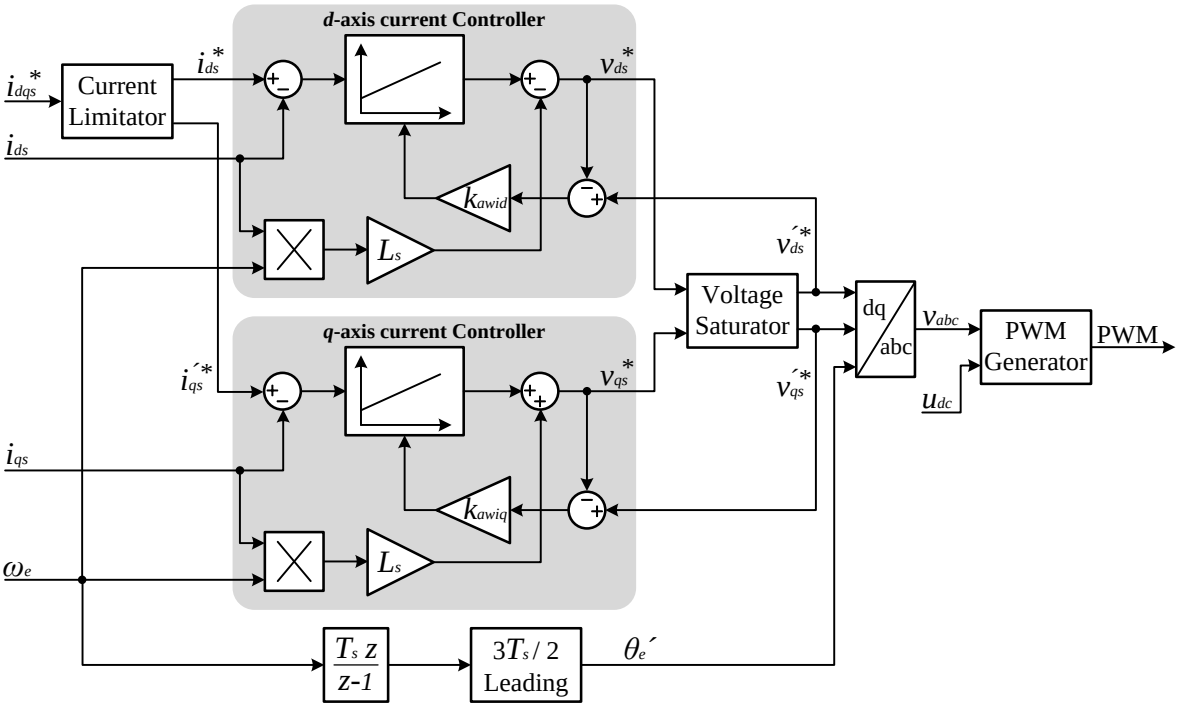


Figure C.11. Current controller block diagram.

As in the previous controllers, *d*-axis and *q*-axis current controllers are based on PI's that transform the current error into a voltage reference that is sent to the PWM modulator. This reference is saturated before its sending to guarantee that the VSC voltage limit is not reached. Both current controllers have anti-windup to minimize the effect of the voltage saturator when it is working.

From equation (C.20), it can be obtained the following:

$$\left.\begin{aligned}\vec{\lambda}_{dqs} &= L_s\,\vec{\imath}_{dqs} + L_m\,\vec{\imath}_{dqr}\\ \vec{\lambda}_{dqr} &= L_r\,\vec{\imath}_{dqr} + L_m\,\vec{\imath}_{dqs}\end{aligned}\right\} \rightarrow\ \vec{\lambda}_{dqs} = \left(L_s - \frac{{L_m}^2}{L_r}\right)\vec{\imath}_{dqs} + \frac{L_m}{L_r}\vec{\lambda}_{dqr} \tag{C.55}$$

Where the notation for complex vector is $\vec{X}_{dq} = \vec{X}_d + j\,\vec{X}_q$. Inserting this notation into the stator voltage-current equation of (C.20), we have the following expression:

$$\vec{V}_{dqs} = (r_s + SL_\sigma + j\omega_e L_\sigma)\,\vec{\imath}_{dqs} + \vec{V}_{ff} \tag{C.56}$$

where S is the Laplace operator, L_σ is the system inductance:

$$L_\sigma = L_s - \frac{{L_m}^2}{L_r} \tag{C.57}$$

and V_{ff} is the feedforward voltage:

$$\vec{V}_{ff} = L_r{}^{-1}(SL_m + \omega_e L_m)\,\vec{\lambda}_{dqr} \tag{C.58}$$

The procedure to obtain the plant transfer function in Laplace domain is based on equation (C.56). As it can be seen, there is not independence between the *d*-axis and the *q*-axis because of the complex term *j*. This effect is known as cross-coupling. Moreover, the feedforward voltage breaks the direct connection between stator current and voltage. For those reasons, it is necessary to make some changes in order to avoid these effects.

The actual plant is given by:

$$T_c(S) = \frac{1}{r_s + SL_\sigma + j\omega_e L_\sigma} \tag{C.59}$$

If the feedforward voltage is removed, and the term $-j\omega_e L_\sigma$ is feed-backed, as it is shown in Figure C.12.a, the following modified plant can be obtained:

$$T_c{}'(S) = \frac{T_c(S)}{1 - j\omega_e L_\sigma T_c(S)} = \frac{1}{r_s + SL_\sigma} \tag{C.60}$$

Now there is a current decoupling, so independent controllers can be used for controlling *d*-axis and *q*-axis current components as shown in Figure C.12.b.

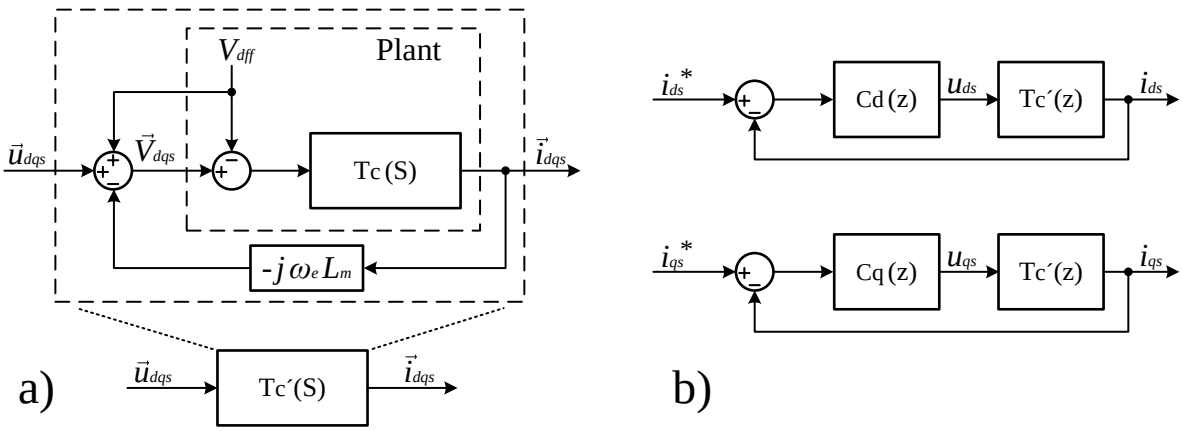


Figure C.12. Procedure to simplify the original plant (a); and independent current controllers closed loops for both components (b).

As shown in diagram of Figure C.11, the feedbacks to achieve the decoupling are inserted. However, the feedforward voltage is not added due to the complexity that it requires and because the behavior of the current controller is not affected at all without it.

The new equivalent plant in the discrete time domain is:

$$T_c'(z) = \frac{a_c}{z - b_c}$$
$$a_c = \frac{1}{r_s}\left(1 - e^{-\frac{r_r'}{L_r'}T_s}\right); \qquad b_c = e^{-\frac{r_r'}{L_r'}T_s} \tag{C.61}$$

Although different current controllers can be implemented for the *d*-axis and *q*-axis, in this case there will be no difference between them: $C_c(z) = C_d(z) = C_q(z)$.

$$H_c(z) = \frac{CT_c'(z)}{1 + CT_c'(z)} = \frac{z - \alpha_c}{z^2 - (1 + b_c - k_{pc}a_c)z + b_c - k_{pc}a_c\alpha_c} \tag{C.62}$$

Once the closed loop transfer function denominator is calculated, it is possible to get the current controller PI constants:

$$k_{pc} = \frac{b_c + 1 - 2e^{-\omega_n \xi T_s}\cos\left(\omega_n\sqrt{1-\xi^2}\,T_s\right)}{a_c}$$
$$\alpha_c = \frac{b_c - e^{-2\omega_n \xi T_s}}{b_c + 1 - 2e^{-\omega_n \xi T_s}\cos\left(\omega_n\sqrt{1-\xi^2}\,T_s\right)} \tag{C.63}$$
$$k_{ic} = \frac{k_{pc}}{T_s}(1 - \alpha_c)$$

And as in the previous controller, the anti-windup gain is chosen as:

$$k_{ac} = \frac{1}{k_{pc}} \tag{C.64}$$

The technique employed to limit the magnitude of the voltage reference when it exceeds the VSC maximum voltage is the Circular Limit method [132]. The principle of this technique is to maintain the angle of the voltage reference vector while the amplitude is reduced when necessary.

The saturated voltage reference vector is transformed into *abc* reference frames. For this task, the electrical stator phase is obtained through the integration of the stator frequency supplied by the FOC. Besides a three half of the sampling period leading is added because of the temporization when this control proposal is test experimentally. *Theta* is calculated in the middle of the current sample period with the measured values of the previous sample period. The actuation for the converter will be sent the next period.

REFERENCES

[1] www.worldenergy.org.

[2] www.eia.gov.

[3] International Energy Outlook 2016. EIA.

[4] Advanced power electronics converters: PWM Converters Processing AC Voltages, Euzeli Cipriano Dos Santos JR., Edison Roberto Cabral Da Silva, IEEE Press, Wiley.

[5] Mohan, N., & Undeland, T. M. (2007). Power electronics: converters, applications, and design. John Wiley & Sons.

[6] Wu, B., & Narimani, M. (2016). High-power converters and AC drives. John Wiley & Sons.

[7] www.appliedmaterials.com.

[8] Trzynadlowski, A. M. (2016). Power electronic converters and systems. The Institution of Engineering and Technology.

[9] Nabae, A., Takahashi, I., & Akagi, H. (1981). A new neutral-point-clamped PWM inverter. IEEE Transactions on industry applications, (5), 518-523.

[10] Chivite-Zabalza, J., Izurza-Moreno, P., Madariaga, D., Calvo, G., & Rodríguez, M. A. (2013). Voltage balancing control in 3-level neutral-point clamped inverters using triangular carrier PWM modulation for FACTS applications. IEEE Transactions on Power Electronics, 28(10), 4473-4484.

[11] Senturk, O. S., Helle, L., Munk-Nielsen, S., Rodriguez, P., & Teodorescu, R. (2011). Converter structure-based power loss and static thermal modeling of the press-pack IGBT three-level ANPC VSC applied to multi-MW wind turbines. IEEE Transactions on Industry Applications, 47(6), 2505-2515.

[12] Tolbert, L. M., Peng, F. Z., & Habetler, T. G. (2000). Multilevel PWM methods at low modulation indices. IEEE Transactions on power electronics, 15(4), 719-725.

[13] Zhou, Y., Jiang, D., Hu, P., Guo, J., Liang, Y., & Lin, Z. (2014). A prototype of modular multilevel converters. IEEE Transactions on Power Electronics, 29(7), 3267-3278.

[14] Holtz, J. (1994). Pulsewidth modulation for electronic power conversion. Proceedings of the IEEE, 82(8), 1194-1214.

[15] Lyu, J., Hu, W., Wu, F., Yao, K., & Wu, J. (2015). Variable modulation offset SPWM control to balance the neutral-point voltage for three-level inverters. IEEE Transactions on Power Electronics, 30(12), 7181-7192.

[16] Narimani, M., Wu, B., & Zargari, N. R. (2016). A novel five-level voltage source inverter with sinusoidal pulse width modulator for medium-voltage applications. IEEE Transactions on Power Electronics, 31(3), 1959-1967.

[17] Perantzakis, G. S., Xepapas, F. H., & Manias, S. N. (2007). A novel four-level voltage source inverter—Influence of switching strategies on the distribution of power losses. IEEE Transactions on Power Electronics, 22(1), 149-159.

[18] Park, Y. M., Yoo, J. Y., & Lee, S. B. (2008). Practical implementation of PWM synchronization and phase-shift method for cascaded H-bridge multilevel inverters based on a standard serial communication protocol. IEEE Transactions on Industry Applications, 44(2), 634-643.

[19] Liang, Y., & Nwankpa, C. O. (1999). A new type of STATCOM based on cascading voltage-source inverters with phase-shifted unipolar SPWM. IEEE Transactions on Industry Applications, 35(5), 1118-1123.

[20] Manias, S., Wiechmann, E. P., & Ziogas, P. D. (1987). Effects of switching angle phase shift on PWM techniques. IEEE Transactions on Industrial Electronics, (4), 463-470.

[21] Celanovic, N., & Boroyevich, D. (2000). A comprehensive study of neutral-point voltage balancing problem in three-level neutral-point-clamped voltage source PWM inverters. IEEE Transactions on power electronics, 15(2), 242-249.

[22] Rojas, R., Ohnishi, T., & Suzuki, T. (1995). An improved voltage vector control method for neutral-point-clamped inverters. IEEE Transactions on Power Electronics, 10(6), 666-672.

[23] Deng, Y., Wang, Y., Teo, K. H., & Harley, R. G. (2016). A simplified space vector modulation scheme for multilevel converters. IEEE Transactions on Power electronics, 31(3), 1873-1886.

[24] Dehghan, S. M., Amiri, A., Mohamadian, M., & Andersen, M. A. (2013). Modular space-vector pulse-width modulation for nine-switch converters. IET Power Electronics, 6(3), 457-467.

[25] Brando, G., Dannier, A., Del Pizzo, A., & Iannuzzi, D. (2013, May). A SVM technique with homopolar voltage control in m-level multi modular converters. In Power Engineering, Energy and Electrical Drives (POWERENG), 2013 Fourth International Conference on (pp. 1531-1537). IEEE.

[26] Xiong, C. L., Wu, X. J., Diao, F., & Feng, X. Y. (2016). Improved nearest level modulation for cascaded H-bridge converter. Electronics Letters, 52(8), 648-649.

[27] Wu, D., & Peng, L. (2016). Characteristics of nearest level modulation method with circulating current control for modular multilevel converter. IET Power Electronics, 9(2), 155-164.

[28] Patel, H. S., & Hoft, R. G. (1973). Generalized techniques of harmonic elimination and voltage control in thyristor inverters: Part I--Harmonic Elimination. IEEE Transactions on Industry Applications, (3), 310-317.

[29] Enjeti, P. N., & Jakkli, R. (1992). Optimal power control strategies for neutral point clamped (NPC) inverter topology. IEEE transactions on industry applications, 28(3), 558-566.

[30] Marzoughi, A., & Imaneini, H. (2013). Optimal selective harmonic elimination for cascaded H-bridge-based multilevel rectifiers. IET Power Electronics, 7(2), 350-356.

[31] Moeini, A., Iman-Eini, H., & Marzoughi, A. (2015). DC link voltage balancing approach for cascaded H-bridge active rectifier based on selective harmonic elimination-pulse width modulation. IET Power Electronics, 8(4), 583-590.

[32] Salimian, H., & Iman-Eini, H. (2016). Fault Tolerant Operation of Three-Phase Cascaded H-Bridge Converters Using an Auxiliary Module. IEEE Transactions on Industrial Electronics.

[33] Moamaei, P., Mahmoudi, H., & Ahmadi, R. (2015, February). Fault-tolerant operation of cascaded H-Bridge inverters using one redundant cell. In Power and Energy Conference at Illinois (PECI), 2015 IEEE (pp. 1-5). IEEE.

[34] Aleenejad, M., Mahmoudi, H., & Ahmadi, R. (2016). Unbalanced space vector modulation with fundamental phase shift compensation for faulty multilevel converters. IEEE Transactions on Power Electronics, 31(10), 7224-7233.

[35] Aleenejad, M., Iman-Eini, H., & Farhangi, S. (2013). Modified space vector modulation for fault-tolerant operation of multilevel cascaded H-bridge inverters. IET Power Electronics, 6(4), 742-751.

[36] Aleenejad, M., Mahmoudi, H., & Ahmadi, R. (2016). A Fault-Tolerant Strategy Based on Fundamental Phase-Shift Compensation for Three-Phase Multilevel Converters With Quasi-Z-Source Networks With Discontinuous Input Current. IEEE Transactions on Power Electronics, 31(11), 7480-7488.

[37] U.S. Patent No. 5986909, Nov. 1999.

[38] Li, K., Yuan, L., Zhao, Z., Lu, S., & Zhang, Y. (2016). Fault-Tolerant Control of MMC with Hot Reserved Submodules Based on Carrier Phase Shift Modulation. IEEE Transactions on Power Electronics.

[39] Briz, F., Lopez, M., Rodriguez, A., & Arias, M. (2016). Modular Power Electronic Transformers: Modular Multilevel Converter Versus Cascaded H-Bridge Solutions. IEEE Industrial Electronics Magazine, 10(4), 6-19.

[40] Klug, R. D., & Klaassen, N. (2005, September). High power medium voltage drives-innovations, portfolio, trends. In Power Electronics and Applications, 2005 European Conference on (pp. 10-pp). IEEE.

[41] Sanchez-Ruiz, A., Mazuela, M., Alvarez, S., Abad, G., & Baraia, I. (2012). Medium voltage–high power converter topologies comparison procedure, for a 6.6 kV drive application using 4.5 kV IGBT modules. IEEE Transactions on Industrial Electronics, 59(3), 1462-1476.

[42] Sanz, I., Bueno, E.J., Rodríguez, F.J., & Moranchel, M. (2014). New Proposal of Switching Strategies for Loss Balancing in ANPC Converters. In Modeling and Simulation of Electric Machines, Converters and Systems, 2014. ELECTRIMACS 2014. 11th International Conference (p. 481-486). IMACS.

[43] Ozpineci, B., Tolbert, L. M., & Chiasson, J. N. (2004, June). Harmonic optimization of multilevel converters using genetic algorithms. In Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual (Vol. 5, pp. 3911-3916). IEEE.

[44] Chiasson, J. N., Tolbert, L. M., McKenzie, K. J., & Du, Z. (2003). Control of a multilevel converter using resultant theory. IEEE Transactions on control systems technology, 11(3), 345-354.

[45] Wells, J. R. (2006). Generalized selective harmonic control (Doctoral dissertation, University of Illinois at Urbana-Champaign).

[46] Bruckner, T., Bernet, S., & Guldner, H. (2005). The active NPC converter and its loss-balancing control. IEEE Transactions on Industrial Electronics, 52(3), 855-868.

[47] Bruckner, T., Bernet, S., & Steimer, P. K. (2007). Feedforward loss control of three-level active NPC converters. IEEE Transactions on Industry Applications, 43(6), 1588-1596.

[48] Andler, D., Alvarez, R., Bernet, S., & Rodriguez, J. (2014). Switching loss analysis of 4.5-kV–5.5-kA IGCTs within a 3L-ANPC phase leg prototype. IEEE Transactions on Industry Applications, 50(1), 584-592.

[49] Deng, Y., Li, J., Shin, K. H., Viitanen, T., Saeedifard, M., & Harley, R. G. (2016). Improved modulation scheme for loss balancing of three-level active NPC converters. IEEE Transactions on Power Electronics.

[50] Pulikanti, S. R., Dahidah, M. S., & Agelidis, V. G. (2011). Voltage balancing control of three-level active NPC converter using SHE-PWM. IEEE Transactions on Power Delivery, 26(1), 258-267.

[51] Pouresmaeil, E., Montesinos-Miracle, D., & Gomis-Bellmunt, O. (2012). Control scheme of three-level NPC inverter for integration of renewable energy resources into AC grid. IEEE systems journal, 6(2), 242-253.

[52] Forrisi, I., Martin, J. P., Nahid-Mobarakeh, B., Petrone, G., Spagnuolo, G., & Pierfederici, S. (2016, September). Stable DC bus voltage balancing in a renewable source grid connected neutral point clamped inverter. In Power Electronics and Motion Control Conference (PEMC), 2016 IEEE International (pp. 1194-1200). IEEE.

[53] Barater, D., Concari, C., Buticchi, G., Gurpinar, E., De, D., & Castellazzi, A. (2016). Performance Evaluation of a Three-Level ANPC Photovoltaic Grid-Connected Inverter With 650-V SiC Devices and Optimized PWM. IEEE Transactions on Industry Applications, 52(3), 2475-2485.

[54] Wang, Y., Shi, W. W., Xie, N., & Wang, C. M. (2014). Diode-free T-type three-level neutral-point-clamped inverter for low-voltage renewable energy system. IEEE Transactions on Industrial Electronics, 61(11), 6168-6174.

[55] Busquets-Monge, S., Ortega, J. D., Bordonau, J., Beristáin, J. A., & Rocabert, J. (2008). Closed-loop control of a three-phase neutral-point-clamped inverter using an optimized virtual-vector-based pulsewidth modulation. IEEE Transactions on Industrial Electronics, 55(5), 2061-2071.

[56] Bueno, E. J., Cobreces, S., Rodríguez, F. J., Hernández, A., Espinosa, F., Mateos, R., ... & López, F. (2005, November). Optimized design of a back-to-back NPC converter to be used as interface for renewable energies. In Industrial Electronics Society, 2005. IECON 2005. 31st Annual Conference of IEEE (pp. 6-pp). IEEE.

[57] Muller, N., Kouro, S., Malinowski, M., Rojas, C. A., Jasinski, M., & Estay, G. (2016). Medium-voltage Power Converter Interface for Multi-generator Marine Energy Conversion Systems. IEEE Transactions on Industrial Electronics.

[58] Yaramasu, V., & Wu, B. (2014). Predictive control of a three-level boost converter and an NPC inverter for high-power PMSG-based medium voltage wind energy conversion systems. IEEE Transactions on Power Electronics, 29(10), 5308-5322.

[59] Li, J., Bhattacharya, S., & Huang, A. Q. (2011). A new nine-level active NPC (ANPC) converter for grid connection of large wind turbines for distributed generation. IEEE transactions on Power Electronics, 26(3), 961-972.

[60] Barros, J. D., & Silva, J. F. (2008). Optimal predictive control of three-phase NPC multilevel converter for power quality applications. IEEE Transactions on Industrial Electronics, 55(10), 3670-3681.

[61] Acuna, P., Morán, L., Rivera, M., Aguilera, R., Burgos, R., & Agelidis, V. G. (2015). A single-objective predictive control method for a multivariable single-phase three-level NPC converter-based active power filter. IEEE Transactions on Industrial Electronics, 62(7), 4598-4607.

[62] Barros, J. D., & Silva, J. F. (2010). Multilevel optimal predictive dynamic voltage restorer. IEEE Transactions on Industrial Electronics, 57(8), 2747-2760.

[63] Saeedifard, M., Nikkhajoei, H., & Iravani, R. (2007). A space vector modulated STATCOM based on a three-level neutral point clamped converter. IEEE Transactions on Power Delivery, 22(2), 1029-1039.

[64] Lin, B. R., & Wei, T. C. (2004). A novel NPC inverter for harmonics elimination and reactive power compensation. IEEE Transactions on Power Delivery, 19(3), 1449-1456.

[65] Madhusoodhanan, S., Mainali, K., Tripathi, A., Patel, D., Kadavelugu, A., Bhattacharya, S., & Hatua, K. (2016). Harmonic Analysis and Controller Design of 15 kV SiC IGBT Based Medium Voltage Grid Connected Three-Phase Three-Level NPC Converter. IEEE Transactions on Power Electronics.

[66] Habibullah, M., Lu, D. D. C., Xiao, D., Fletcher, J. E., & Rahman, M. F. (2016). Predictive Torque Control of Induction Motor Sensorless Drive Fed by a 3L-NPC Inverter. IEEE Transactions on Industrial Informatics.

[67] Choudhury, A., Pillay, P., & Williamson, S. S. (2015). A hybrid PWM-based DC-link voltage balancing algorithm for a three-level NPC DC/AC traction inverter drive. IEEE Journal of Emerging and Selected Topics in Power Electronics, 3(3), 805-816.

[68] Mohan, D., Zhang, X., & Foo, G. H. B. (2016). Three-Level Inverter-Fed Direct Torque Control of IPMSM With Torque and Capacitor Voltage Ripple Reduction. IEEE Transactions on Energy Conversion, 31(4), 1559-1569.

[69] Madishetti, S., Singh, B., & Bhuvaneswari, G. (2016). Three-Level NPC-Inverter-Based SVM-VCIMD With Feedforward Active PFC Rectifier for Enhanced AC Mains Power Quality. IEEE Transactions on Industry Applications, 52(2), 1865-1873.

[70] Zaragoza, J., Pou, J., Ceballos, S., Robles, E., Jaen, C., & Corbalan, M. (2009). Voltage-balance compensator for a carrier-based modulation in the neutral-point-clamped converter. IEEE Transactions on Industrial Electronics, 56(2), 305-314.

[71] Yazdani, A., & Iravani, R. (2010). Voltage-sourced converters in power systems: modeling, control, and applications. John Wiley & Sons.

[72] Abu-Rub, H., Holtz, J., Rodriguez, J., & Baoming, G. (2010). Medium-voltage multilevel converters—State of the art, challenges, and requirements in industrial applications. IEEE Transactions on Industrial Electronics, 57(8), 2581-2596.

[73] Gupta, A. K., & Khambadkone, A. M. (2006). A space vector PWM scheme for multilevel inverters based on two-level space vector PWM. IEEE Transactions on industrial electronics, 53(5), 1631-1639.

[74] Wei, S., Wu, B., Li, F., & Liu, C. (2003, February). A general space vector PWM control algorithm for multilevel inverters. In Applied Power Electronics Conference and Exposition, 2003. APEC'03. Eighteenth Annual IEEE (Vol. 1, pp. 562-568). IEEE.

[75] Sozer, Y., Torrey, D. A., Saha, A., Nguyen, H., & Hawes, N. (2014). Fast minimum loss space vector pulse-width modulation algorithm for multilevel inverters. IET Power Electronics, 7(6), 1590-1602.

[76] Seo, J. H., Choi, C. H., & Hyun, D. S. (2001). A new simplified space-vector PWM method for three-level inverters. IEEE Transactions on power electronics, 16(4), 545-550.

[77] Deng, Y., Teo, K. H., Duan, C., Habetler, T. G., & Harley, R. G. (2014). A fast and generalized space vector modulation scheme for multilevel inverters. IEEE Transactions on Power Electronics, 29(10), 5204-5217.

[78] Jacob, B., & Baiju, M. R. (2015). A new space vector modulation scheme for multilevel inverters which directly vector quantize the reference space vector. IEEE Transactions on Industrial Electronics, 62(1), 88-95.

[79] Castro, L. G., Correa, M. B., Jacobina, C. B., & Boroyevich, D. (2010, September). A fast space-vector algorithm for multilevel converters without coordinates transformation. In Energy Conversion Congress and Exposition (ECCE), 2010 IEEE (pp. 2543-2547). IEEE.

[80] AS, A. M., Gopinath, A., & Baiju, M. R. (2009). A simple space vector PWM generation scheme for any general n-level inverter. IEEE Transactions on Industrial Electronics, 56(5), 1649-1656.

[81] Correa, P., Pacas, M., & Rodriguez, J. (2006, July). Modulation strategies for fault-tolerant operation of H-bridge multilevel inverters. In Industrial Electronics, 2006 IEEE International Symposium on (Vol. 2, pp. 1589-1594). IEEE.

[82] Wei, S., Wu, B., Li, F., & Sun, X. (2003, February). Control method for cascaded H-bridge multilevel inverter with faulty power cells. In Applied Power Electronics Conference and Exposition, 2003. APEC'03. Eighteenth Annual IEEE (Vol. 1, pp. 261-267). IEEE.

[83] Paymani, M. A., Marhaba, M. S., & Iman-Eini, H. (2011, February). Fault-tolerant operation of a medium voltage drive based on the Cascaded H-bridge inverter. In Power Electronics, Drive Systems and Technologies Conference (PEDSTC), 2011 2nd (pp. 551-556). IEEE.

[84] Lezana, P., Ortiz, G., & Rodríguez, J. (2008, August). Operation of regenerative cascade multicell converter under fault condition. In Control and Modeling for Power Electronics, 2008. COMPEL 2008. 11th Workshop on (pp. 1-6). IEEE.

[85] Song, W., & Huang, A. Q. (2010). Fault-tolerant design and control strategy for cascaded H-bridge multilevel converter-based STATCOM. IEEE Transactions on Industrial Electronics, 57(8), 2700-2708.

[86] Lezana, P., & Ortiz, G. (2009). Extended operation of cascade multicell converters under fault condition. IEEE Transactions on Industrial Electronics, 56(7), 2697-2703.

[87] Hammond, P. W. (1997). A new approach to enhance power quality for medium voltage AC drives. IEEE Transactions on Industry Applications, 33(1), 202-208.

[88] Cecati, C., Ciancetta, F., & Siano, P. (2010). A multilevel inverter for photovoltaic systems with fuzzy logic control. IEEE Transactions on Industrial Electronics, 57(12), 4115-4125.

[89] Ng, C. H., Parker, M. A., Ran, L., Tavner, P. J., Bumby, J. R., & Spooner, E. (2008). A multilevel modular converter for a large, light weight wind turbine generator. IEEE Transactions on Power Electronics, 23(3), 1062-1074.

[90] Liang, X., & He, J. (2016). Load Model for Medium Voltage Cascaded H-Bridge Multi-Level Inverter Drive Systems. IEEE Power and Energy Technology Systems Journal, 3(1), 13-23.

[91] Khoucha, F., Lagoun, M. S., Kheloui, A., & Benbouzid, M. E. H. (2011). A comparison of symmetrical and asymmetrical three-phase H-bridge multilevel inverter for DTC induction motor drives. IEEE Transactions on Energy Conversion, 26(1), 64-72.

[92] Nagata, K., Okuyama, T., Nemoto, H., & Katayama, T. (2008). A simple robust voltage control of high power sensorless induction motor drives with high start torque demand. IEEE Transactions on Industry Applications, 44(2), 604-611.

[93] Kandasamy, K., Vilathgamuwa, M., & Tseng, K. J. (2015). Inter-module state-of-charge balancing and fault-tolerant operation of cascaded H-bridge converter using multi-dimensional modulation for electric vehicle application. IET Power Electronics, 8(10), 1912-1919.

[94] Khoucha, F., Lagoun, S. M., Marouani, K., Kheloui, A., & Benbouzid, M. E. H. (2010). Hybrid cascaded H-bridge multilevel-inverter induction-motor-drive direct torque control for automotive applications. IEEE Transactions on Industrial Electronics, 57(3), 892-899.

[95] Amini, J., & Moallem, M. (2016, October). A capacitor voltage balancing method for cascaded H-bridge multilevel inverters with application to FACTS. In Industrial Electronics Society, IECON 2016-42nd Annual Conference of the IEEE (pp. 6447-6452). IEEE.

[96] Nie, S., Mao, C., & Wang, D. (2016, October). Fault tolerant design for electronic power transformer. In Power and Energy Engineering Conference (APPEEC), 2016 IEEE PES Asia-Pacific (pp. 692-696). IEEE.

[97] Behrouzian, E., & Bongiorno, M. (2017). Investigation of Negative-Sequence Injection Capability of Cascaded H-Bridge Converters in Star and Delta Configuration. IEEE Transactions on Power Electronics, 32(2), 1675-1683.

[98] Song, W., & Huang, A. Q. (2010). Fault-tolerant design and control strategy for cascaded H-bridge multilevel converter-based STATCOM. IEEE Transactions on Industrial Electronics, 57(8), 2700-2708.

[99] Chavan, G., & Bhattacharya, S. (2016, October). A novel control algorithm for a static series synchronous compensator using a Cascaded H-bridge converter. In Industry Applications Society Annual Meeting, 2016 IEEE (pp. 1-6). IEEE.

[100] Perez, M. A., Bernet, S., Rodriguez, J., Kouro, S., & Lizana, R. (2015). Circuit topologies, modeling, control schemes, and applications of modular multilevel converters. IEEE transactions on power electronics, 30(1), 4-17.

[101] Nami, A., Liang, J., Dijkhuizen, F., & Demetriades, G. D. (2015). Modular multilevel converters for HVDC applications: Review on converter cells and functionalities. IEEE Transactions on Power Electronics, 30(1), 18-36.

[102] António-Ferreira, A., & Gomis-Bellmunt, O. (2016, June). Comparison of cell selection methods for modular multilevel converters. In Environment and Electrical Engineering (EEEIC), 2016 IEEE 16th International Conference on (pp. 1-8). IEEE.

[103] Li, B., Yang, R., Xu, D., Wang, G., Wang, W., & Xu, D. (2015). Analysis of the phase-shifted carrier modulation for modular multilevel converters. IEEE Transactions on Power Electronics, 30(1), 297-310.

[104] Gowaid, I. A., Adam, G. P., Ahmed, S., Holliday, D., & Williams, B. W. (2015). Analysis and design of a modular multilevel converter with trapezoidal modulation for medium and high voltage dc-dc transformers. IEEE Transactions on Power Electronics, 30(10), 5439-5457.

[105] Konstantinou, G., Ciobotaru, M., & Agelidis, V. (2013). Selective harmonic elimination pulse-width modulation of modular multilevel converters. IET Power Electronics, 6(1), 96-107.

[106] Moranchel, M., Bueno, E., Sanz, I., & Rodríguez, F. J. (2017). New Approaches to Circulating Current Controllers for Modular Multilevel Converters. Energies, 10(1), 86.

[107] Francos, P. L., Verdugo, S. S., Álvarez, H. F., Guyomarch, S., & Loncle, J. (2012, July). INELFE—Europe's first integrated onshore HVDC interconnection. In Power and Energy Society General Meeting, 2012 IEEE (pp. 1-8). IEEE.

[108] Deng, Y., & Harley, R. G. (2015). Space-vector versus nearest-level pulse width modulation for multilevel converters. IEEE transactions on power electronics, 30(6), 2962-2974.

[109] Moranchel, M., Bueno, E. J., Rodriguez, F. J., & Sanz, I. (2014, October). Novel capacitor voltage balancing algorithm for modular multilevel converter. In Industrial Electronics Society, IECON 2014-40th Annual Conference of the IEEE (pp. 4697-4701). IEEE.

[110] Akagi, H. (2011). Classification, terminology, and application of the modular multilevel cascade converter (MMCC). IEEE Transactions on Power Electronics, 26(11), 3119-3130.

[111] Glinka, M., & Marquardt, R. (2005). A new AC/AC multilevel converter family. IEEE Transactions on Industrial Electronics, 52(3), 662-669.

[112] Khan, F. H., & Tolbert, L. M. (2007). A multilevel modular capacitor-clamped DC–DC converter. IEEE Transactions on Industry Applications, 43(6), 1628-1638.

[113] Saeedifard, M., & Iravani, R. (2010). Dynamic performance of a modular multilevel back-to-back HVDC system. IEEE Transactions on power delivery, 25(4), 2903-2912.

[114] Zhao, B., Song, Q., Li, J., Wang, Y., & Liu, W. (2016). High-Frequency-Link Modulation Methodology of DC-DC Transformer Based on Modular Multilevel Converter for HVDC

Application: Comprehensive Analysis and Experimental Verification. IEEE Transactions on Power Electronics.

[115] Oliveira, R., & Yazdani, A. (2017). A Modular Multilevel Converter With DC Fault Handling Capability and Enhanced Efficiency for HVdc System Applications. IEEE Transactions on Power Electronics, 32(1), 11-22.

[116] Hao, Q., Ooi, B. T., Gao, F., Wang, C., & Li, N. (2016). Three-phase series-connected modular multilevel converter for HVDC application. IEEE Transactions on Power Delivery, 31(1), 50-58.

[117] Oates, C. (2015). Modular multilevel converter design for VSC HVDC applications. IEEE Journal of Emerging and Selected Topics in Power Electronics, 3(2), 505-515.

[118] Parker, M. A., Ng, C., & Ran, L. (2011). Fault-tolerant control for a modular generator–converter scheme for direct-drive wind turbines. IEEE Transactions on Industrial Electronics, 58(1), 305-315.

[119] Wang, M., Hu, Y., Zhao, W., Wang, Y., & Chen, G. (2016). Application of modular multilevel converter in medium voltage high power permanent magnet synchronous generator wind energy conversion systems. IET Renewable Power Generation, 10(6), 824-833.

[120] Parastar, A., Kang, Y. C., & Seok, J. K. (2015). Multilevel modular dc/dc power converter for high-voltage dc-connected offshore wind energy applications. IEEE Transactions on Industrial electronics, 62(5), 2879-2890.

[121] Soong, T., & Lehn, P. W. (2014). Evaluation of emerging modular multilevel converters for BESS applications. IEEE Transactions on Power Delivery, 29(5), 2086-2094.

[122] Du, S., & Liu, J. (2013). A study on dc voltage control for chopper-cell-based modular multilevel converters in D-STATCOM application. IEEE Transactions on Power Delivery, 28(4), 2030-2038.

[123] Xu, C., Dai, K., Chen, X., & Kang, Y. (2016). Voltage droop control at point of common coupling with arm current and capacitor voltage analysis for distribution static synchronous compensator based on modular multilevel converter. IET Power Electronics, 9(8), 1643-1653.

[124] Bina, M. T. (2011). A transformerless medium-voltage STATCOM topology based on extended modular multilevel converters. IEEE Transactions on Power Electronics, 26(5), 1534-1545.

[125] Li, B., Zhou, S., Xu, D., Yang, R., Xu, D., Buccella, C., & Cecati, C. (2016). An improved circulating current injection method for modular multilevel converters in variable-speed drives. IEEE Transactions on Industrial Electronics, 63(11), 7215-7225.

[126] Li, B., Zhou, S., Xu, D., Finney, S., & Williams, B. (2016). A Hybrid Modular Multilevel Converter for Medium-Voltage Variable-Speed Motor Drives. IEEE Transactions on Power Electronics.

[127] Tai, B., Gao, C., Liu, X., & Chen, Z. (2017). A Novel Flexible Capacitor Voltage Control Strategy for Variable-Speed Drives With Modular Multilevel Converters. IEEE Transactions on Power Electronics, 32(1), 128-141.

[128] He, L., Zhang, K., Xiong, J., Fan, S., & Xue, Y. (2016). Low-Frequency Ripple Suppression for Medium-Voltage Drives Using Modular Multilevel Converter With Full-Bridge Submodules. IEEE Journal of Emerging and Selected Topics in Power Electronics, 4(2), 657-667.

[129] Ottersten, R. (2003). On control of back-to-back converters and sensorless induction machine drives. Chalmers University of Technology.

[130] Chee, M. (1998). Dynamic simulation of electric machinery.

[131] Vas, P. (1998). Sensorless vector and direct torque control. Oxford Univ. Press.

[132] Ottersten, R., & Svensson, J. (2002). Vector current controlled voltage source converter-deadbeat control and saturation strategies. IEEE Transactions on Power Electronics, 17(2), 279-285.